Data Analysis Report

Virtex-7

Architectural Features

SEU Characterization Summary

– In-beam dynamic testing on Xilinx 7-Series FPGA family –

(Placeholder for editors)

DRAFT

Changes Control table

Rev.	Date	Responsible	Brief description
A	2020·03·01	G. M. Swift *et al.*	Initial release.

Xilinx Space Policy for non-XQR Parts

It is the stated policy of Xilinx to only provide radiation performance data, guidance or support for the use of Xilinx products in Space Radiation Environment applications for products designated as Xilinx Space (XQR) products. As such, Xilinx will not provide this type of data, guidance or support for non-XQR products. The Space Radiation Environment is a branch of astronautics, aerospace engineering and space physics that seeks to understand and address conditions existing in space that affect the design and operation of spacecraft, launch vehicles and associated electronic systems. Only Xilinx Space (XQR) products are specified and endorsed for use in the space environment. The Xilinx standard terms and conditions state that the Xilinx Limited Warranty does not apply to and excludes to the maximum extent permitted by applicable law “Products used in an application or environment that is not within the Specifications”. Customers choosing to use Xilinx products in space environments that are not specified for use in space do so entirely at their own risk.

Xilinx continues to support the Xilinx Radiation Test Consortium (XRTC) activities. Xilinx does post the proceedings from the XRTC annual meeting in the Xilinx Space Lounge, by prior agreement with the Consortium. Do note that the XRTC is a distinct and separate organization from Xilinx.

The chairperson for the XRTC is Gary Swift, who can be contacted via the information below:

Gary M. Swift
Swift Engineering and Radiation Services, LLC.
Phone: +1 408-628-4803 (landline) or +1 408-679-3785 (cell)
E-mail: gary.m.swift@ieee.org

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Contents

1 Purpose and Scope

The use of commercial reconfigurable Field-Programmable Gate Arrays (FPGAs) instead of custom Application-Specific Integrated Circuits (ASICs) has become increasingly becoming increasingly more attractive, especially for spacecraft avionics. Reconfigurable FPGAs can offer improvements on a variety of operational aspects after deployment, including mission-saving situations, dynamic adaptation to shifting performance needs during different mission phases. This “Flexibility Advantage” can be enabled through a variety of means, e.g., through on-orbit design changes via uploads, by launching a spacecraft with several alternative design variants, or the use of a spacecraft-internal central or distributed reconfiguration facilities. The “Flexibility Advantage” is sometimes not realized due to institutional barriers and reluctance to deploy such flexible avionics architectures in space systems.

FPGAs offer also what can be referred to as the “traditional FPGA Advantage” Ever since reaching technological maturity, programmable logic devices have held a clear advantage over ASICs especially regarding development time and cost as well as manpower requirements. At a minimum, their use over ASICs can allow for at least $2\times$ faster initial test development and two orders of magnitude for re-spins of existing designs, which can be achieved within hours or days instead of months or years. On the other hand, as compared to FPGAs, ASICs excel in terms of achievable clock speeds, reduced signal latency, lower power consumption due to circuit- and transistor-level customization, and overall design freedom. The “traditional FPGA Advantage” today makes reconfigurable logic devices attractive despite the performance advantages offered by custom ASICs. However, these ASIC advantages only hold when comparing identical technology nodes. The performance-gap between FPGAs and ASICs shrinks drastically with feature size and maturity of the used technology nodes. Considering the development time required for ASIC-based setups, there often exists a break-even point exists where performance balance is level or even tilted towards FPGA devices. Certainly, this point is reached when considering FPGAs that are two or more nodes ahead of ASICs, e.g., comparing 65 nm ASIC with 28 nm FPGAs such as a Xilinx Series-7 device.

However, today the radiation susceptibility of a specific FPGA generation is a major concern in space systems engineering and avionics design, transcending any FPGA advantage. At the time of writing, concerns over component reliability and behavior under radiation occasionally still trump considerations regarding cost, efficiency, component survivability, and mission saving potential. The Xilinx Radiation Test Consortium (XRTC), an association of interested aerospace entities including leading aerospace companies, universities, space agencies and national laboratories, pools resources in order to characterize the behavior of modern FPGAs and bound those concerns with clear data.

Over the past four years, the XRTC and others have characterized the static Single-Event Upset (SEU) and Single-Event Latch-up (SEL) susceptibility of Xilinx’ 28 nm (*7-Series*) and 20 nm (*UltraScale*) FPGAs, both based on planar high-κ dielectric and metal gate (HKMG) processes; those radiation effects results were presented and published, notably at the NSREC, RADECS and MAPLD conferences, the SEE Symposium, as well as the XRTC Annual Meetings [1–6]. Recently, the consortium has measured Single-Event Effects (SEEs) rates on selected *7-Series* features that require in-beam clocking – that is, in-beam dynamic testing. The results are described in detail within this report, expanding the preliminary results presented as a *late news* posters and manuscript in the Radiation-Effects Data Workshop (REDW) session at RADECS 2017 conference [7].

2 Data Analysis Team

Beam test data and results were analyzed by William Rowe (BRAM, SEFIs), Kevin Wray (CMT), Sebastián García (IOB), Gary Swift (all types) and Christian M. Fuchs. Sample thickness analysis and LET assignment were performed by Gary Swift, William Rowe and Sebastián García, also with a preliminary contribution of Stephen Stone (Lockheed-Martin Space Systems). Report and Virtex-7 primitive result analysis texts reworked and editing by Christian M. Fuchs. In general, all team members contributed and cross-reviewed on most topics.

Austin Lesea (Lockheed-Martin Space Systems) contributed on specific device architecture topics. Krysten Pfau (Raytheon Space and Airborne Systems) participated on an early stage of the IOSERDES data analysis process. Gary Swift was involved in all aspects of the data analysis.

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4 Acronyms and Abbreviations

ASIC Application-Specific Integrated Circuit

BBPM *Block RAM* bit position modification

BGA Ball Grid Array

BRAM Block Random-Access Memory

CI Cyclotron Institute

CMT Clock Management Tile

CNL Crocker Nuclear Laboratory

ConfigMon Configuration Monitor

CRAM Configuration Random-Access Memory

CTI Common Test Infrastructure

DCM Digital Clock Manager

DSP Digital Signal Processing

DUT Device Under Test

ECC Error Correcting Code

EDAC Error Detection and Correction

F/F Flip-flop

FPGA Field-Programmable Gate Array

FuncMon Functional Monitor

GEO Geostationary Earth Orbit

GUI Graphical User Interface

HDL Hardware Description Language

HKMG high-κ dielectric and metal gate

HSTL High Speed Transceiver Logic

I/O Input/Output

IOB Input-Output Block

IP Intellectual Property module

JCM JTAG Configuration Manager

JPL Jet Propulsion Laboratory

JTAG Joint Test Action Group (IEEE stds. 1149 and 1532)

LET Linear Energy Transfer

LVCMOS Low-Voltage Complementary Metal-Oxide-Semiconductor

LVTTL	Low-Voltage TTL
LVDS	Low-Voltage Differential Signaling
MAPLD	Military & Aerospace Programmable Logic Devices workshop
MBU	Multiple-Bit Upset
MCU	Multiple-Cell Upset
MMCM	Mixed-Mode Clock Manager
NASA	National Aeronautics and Space Administration
NSREC	Nuclear & Space Radiation Effects Conference
PCIe	Peripheral Component Interconnect Express interface
PLL	Phase-Locked Loop
RADECS	Radiation and its Effects on Components and Systems
REDW	Radiation-Effects Data Workshop
SECDED	Single-Error Correction and Double-Error Detection
SEE	Single-Event Effect
SEFI	Single-Event Functional Interrupt
SEL	Single-Event Latch-up
SET	Single-Event Transient
SEU	Single-Event Upset
SEUSS	Single Event Upset System Supervisor
SRIM	Stopping and Range of Ions in Matter
TAMU	Texas A&M University
UCD	University of California, Davis
V-5QV	Virtex-5QV
XRTC	Xilinx Radiation Test Consortium
HR	high-range
HP	high-performance

5 Notation and Units

In all Weibull fits, units for the saturation cross-section σ_{sat} parameter are $\left[\text{cm}^2/\text{resource}\right]$, unless otherwise noted. A “resource” refers the actual resource under test, e.g. BRAM blocks or an MMCM/PLL element. Units for the LET threshold L_{th} and width W parameters are $\left[\text{MeV cm}^2/\text{mg}\right]$. The color of Weibull fit curves are plotted with matching colors to experimentally-obtained points including error bars. Elements that are plotted entirely as error bars indicate results with insufficient data.

6 Overview

The *Virtex-7* FPGA generation offers an abundance of powerful and complex architectural features. Due to the large number of programmable features and available options, the conducted tests and parameters, as well as the associated data analysis can be quite complex. Due to necessity, the test matrices alone cannot provide full coverage of all possible operating modes.

In this Architectural Features Summary, we therefore limit ourselves to report at a high level on: **a)** the **features or blocks of interest** that were tested, **b)** the **test methodology** employed, and **c)** the **most important results** obtained, as well as, **d)** where relevant, **significant observations** made while executing tests or analyzing test data. Our objective is therefore to provide **all necessary information** and data to **calculate expected** and/or **worst-case SEE rates** for the relevant, parametrized for specific on-orbit radiation environments as reference. It is our hope that this data will help that identifying and quantifying the main error modes within the FPGA generation will inspire novel mitigation ideas for the Consortium to test.

More complete documentation on the blocks tested is available within the relevant Virtex-7 User Guides provided by Xilinx. Many of the radiation-testing related documents collected in the References section (§3) are available on the Jet Propulsion Laboratory (JPL)'s Radiation Effects on FPGA website [8]. Alternatively, due to current maintenance activities on the JPL-NASA site, Xilinx' space industry customers can access these documents on the Space Lounge site [9].

7 Test Campaign Setup and Parameters

7.1 Test Infrastructure Setup

The test approach leveraged the XRTC's Common Test Infrastructure (CTI) apparatus and several targeted mature test and monitoring designs (or IP) previously developed under XRTC auspices. These had been developed for and used during SEE dynamic testing campaigns for previous generation Xilinx FPGAs. Most recently and most extensively, the CTI was utilized for testing the 65 nm *Virtex-5QV* device family [10, 11].

The high-level architecture of the CTI setup used during this test campaign is depicted in figure **??** (reprinted from [10]). The CTI consists of a mature custom test backplane (Generation-2 motherboard) functioning as carrier for tailored daughter cards. This test setup has already been used by the consortium to characterize 4 prior generations of Xilinx FPGAs. **[Gary]: Virtex 2 Pro, V5QV, and which others?** The Gen2 CTI consists of one in-beam FPGA and two out-of-beam service FPGAs: **a)** The in-beam Device Under Test (DUT) card, holding the actual FPGA to be tested, **b)** an out-of-beam Virtex 2 Pro FPGA, *ConfigMon*, monitor and scrub the DUT's running configuration for CRAM upsets and monitor/recovery from SEFIss, and **c)** an out-of-beam Virtex 2 Pro FPGA, *FuncMon*, which controls the design implemented on the target DUT during a radiation test for functional errors and other failures.

ConfigMon and *FuncMon* operate independently of each other and acquire DUT-related data independently. Both the Configuration Monitor (ConfigMon) and the Functional Monitor (FuncMon) stream real-time data out of the target room, where it is received, processed, and logged disk in text-based strip-chart files. Monitoring was done using a version of the XRTC's standard GUIs application suite. During several test runs with V7-585T parts and all test runs with V7-980T devices, a *ConfigMon* alternative developed by BYU was utilized to augment capabilities that FuncMon lacked (see Section 7.3).

The XRTC CTI uses dedicated lab power supplies for each DUT power rail. Currents and voltages for each rail are routinely recorded as log files plot-able as strip-charts. The software responsible for this logging is also is responsible handling high-current latchups and other power-related anomalies, and will cycle power if such an event is detected.

7.2 Device Under Test Specifications

To provide test results as accurate and as representative for the entire *Virtex-7* FPGA family as possible, the largest monolithic *Virtex-7* device was chosen. Specifically, the radiation tests were carried out with the FPGA component part number XQ7VX980TRF1930ABX1637packaged in flip-chip Ball Grid Arrays (BGAs), which is henceforth referred to as DUT. Six DUTs were soldered onto copies of a custom DUT carrier cards (DUT cards). Five of these DUTs these were de-lidded. Of these, three were thinned to less than 100 µm residual silicon substrate via mechanical milling. All DUTs used in this test campaign were purchased from a single wafer lot, with log code being DD5284886A.

Intermediately while the V7-980T DUT card was being designed and manufactured, three unirradiated samples of a smaller *Virtex-7* devices, XC7V585T, were utilize as well. These components had been soldered to pre-existing DUT cards and were delidded and thinned < 100 µm. Details of the specific devices and features tested are given in Tables 1 and 2.

Table 1: The *Virtex-7* DUTs utilized used to obtain the radiation test results within the report.

Device	Total	De-lidded	Thinned	Same Lot?	Wafer Lot No.
XQ7VX980T	6	5	3	yes	DD5284886A
XC7V585T	3	3	3	yes	unknown

Table 2: Selected Architectural Features of Target *Virtex-7* Devices

	XC7V585T		**XQ7VX980T**	
Resource	Total	Tested	Total	Tested
MMCM	18	4	18	4
PLL	18	4	18	4
BRAM with ECC	795	795	1500	795
IOB (HR)	100	80	–	–
IOB (HP)	750	–	900	213

7.3 Evolution of Test IP since Virtex-5QV

Due to architectural differences between the Series-5 and Series-7 generation devices, a direct reuse of Virtex-5 designs for DUT, *ConfigMon*, and *FuncMon* is not possible. Furthermore, while designs for Virtex-5QV devices were developed using Xilinx ISE Design Suite, Series-7 and newer generation FPGAs are covered by Xilinx's Vivado Design Suit. In this section, we therefore discuss adaptations and enhancements made to the CTI as compared to the Virtex-5QV characterization report.

The V-5QV *ConfigMon* design was extended and adapted to work with the *Virtex-7* family, and tailored for the V7-980T device. This design was capable of counting the number of configuration bits upsets and sampling a limited number of the relevant CRAM locations. The *ConfigMon* design was modified to keep the DUT's configuration bitstream in NAND flash. This was necessary because the size of the V7-980T bitstream (almost 250 Mbit) exceeded the capacity of the XRTC non-volatile PROM card. This changed the readback/scrub cycle

time to approximately 6.7 seconds due to performance limitations of the 16/33Mhz-clocked SMAP interface. All V7-980T and V7-585T test runs were carried out with this *ConfigMon* design.

JCM, a BYU developed *ConfigMon* alternative, was used during V7-980T test runs at TAMU in March 2017. It was used to capture the full configuration bitstream sampled from the DuT card, instead of just monitoring the DUT's CRAM. This design was based on a Zynq/ARM-based JTAG module connected to the Gen2 Motherboard via Ethernet, and had been used for static testing in earlier test campaigns [1–3]. In contrast to *ConfigMon*, this design was limited to a readback-cycle duration of approximately 15 seconds and a scrub-cycle duration of 25 seconds.

7.4 Features Under Test

Modern FPGAs are more than just a programmable fabric and including many ASIC-like useful. These form highly flexible sub-circuits that are stitched together by an application designer using the configurable logic, flip-flops and routing-network of the configurable fabric. Six of the most important resources present within a Virtex-7 FPGA are:

- **IOB** – Input/Output Blocks, and
- **IOB-FF** – an optional register associated with IOB, as well as their
- **SERDES** – optional serializer-deserializer components for IOBs.
- **BRAM** – *Block RAM* user SRAM blocks, and
- **BRAM-ECC** – the error-correcting circuit attached to BRAM implementing optional hamming-coding.
- **MMCM** – the digital-locked loop based mixed-mode clock and clock management blocks, and
- **PLL** – the phase-locked loop clocking blocks.

This characterization report contains data on all these components, which were subjected to radiation testing in several test campaigns, so that a variety of in-beam dynamic SEE measurements could be taken.

The DUT and *FuncMon* HDL designs previously used for testing *Virtex-5QV* IOB and BRAM-ECC were ported to the V7-585T, and for each of the six selected features were ported to the V7-980T. For comparison purposes, the BRAM IP was also ported to the two *Virtex-7* DUTs. An overview of each of these feature test designs and methodology is given in the corresponding sections of Ref. [11].

7.5 Test Campaign Chronology

The *Virtex-7* test campaign consisted of three separate beam trips, with a total of four trips planned. Two heavy ion tests were conducted in the Texas A&M University (TAMU) cyclotron (CI). In addition, one proton test was conducted using the University of California, Davis (UCD) cyclotron (CNL). The following run sequence with the following devices, radiation types, and resources were carried out:

1. A heavy ion radiation test was conducted in December 2016 using the pre-existing V7-585T DUT cards. During this test run the following resources were tested: LVCMOS-IOB, BRAM, and BRAM-ECC. The BRAM-ECC test design was discovered to be dysfunctional during the beam trip, so no data was generated for this primitive.
2. A proton test run was conducted in January 2017, this time using the now available V7-980T DUT cards. During this test run the following resources were tested: LVDS-IOB, LVCMOS-IOB, BRAM, and BRAM-ECC.

3. A heavy ion test on newly available V7-980T DUT cards was conducted in March 2017. During this test run the following resources were tested: LVDS-IOB, LVCMOS-IOB, HSTL-IOB, IOB Banks, SERDES, BRAM, and BRAM-ECC.

Both heavy ion tests and the proton test were performed in-air. Beam details are given in Table 3. The acquired data allows reasonable accurate calculation of space upset rates for the *Virtex-7* features-under-test.

The third test run was highly successful, and a sufficient amount of data had been collected. This resulted in the decision to cancel a planned fourth radiation test under heavy ions, that had been scheduled for April 2017. While the obtained data set was therefore sufficient, this decision resulted in some 'gaps' in the V7 characterization report's dataset. These however effects specifically the very high LETs range, that a 15 MeV/u ^{129}Xe ion would have provided.

A test designs for characterizing IOB IDELAY/ODELAY behavior under radiation was developed as well, but became available only after the March 2017 beam trip. At that point in time, the design was considered beam-ready and functional. As a consequence of the cancellation of the April 2017 beam trip, the scheduled IDELAY/ODELAY test runs went unfilled, which was deemed acceptable. However, during subsequent data analysis, it was discovered that only a limited amount of valid data data had been generated for IOB resources overall. This constraints the accuracy with which the Virtex-7 IOB behavior can be characterized. At the time of writing this report, there is interest with some consortium partners, space companies, to conduct follow up tests on this aspect. Therefore, if and when resources to conduct these tests become available in the future, a complementary test of the mentioned primitives will be conducted. This may also provide an opportunity to test other interesting blocks (*e.g.,* user F/F, DSP behavior, and the PCIe IP.

Table 3: Test Campaign Summary

Type	Facility	Date	Energy	Ion Species
Heavy ions	TAMU	Dec. 2016	24.8 MeV/u	^{14}N, ^{40}Ar, ^{84}Kr
Protons	UCD	Jan. 2017	63 MeV	–
Heavy ions	TAMU	Mar. 2017	24.8 MeV/u	^{40}Ar, ^{84}Kr
			40 MeV/u	^{14}N, ^{20}Ne

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8 Die Thickness and LET Assignment

An ion beam can not penetrate the entire active region of the silicon of a V7-DUT's die. Hence, the flip-chip packaging of the utilized V7-DUTs necessitates backside thinning to produce representative results during heavy ion tests. This can be done through a variety of measures, and in this test campaign mechanical milling was chosen. The actual die thickness of the DUT affects LET assignments, and therefore must be considered. However, this process does not produce 100% identical results for all processed dies. In this section, we will therefore discuss die thickness measurements for the utilized V7-DUTs.

V5-585T DUTs were thinned & polished by Jim Colvin of FA Instruments, Inc., with thickness variations being indicated in Fig. 1 [CF to Gary: anywhere published?].

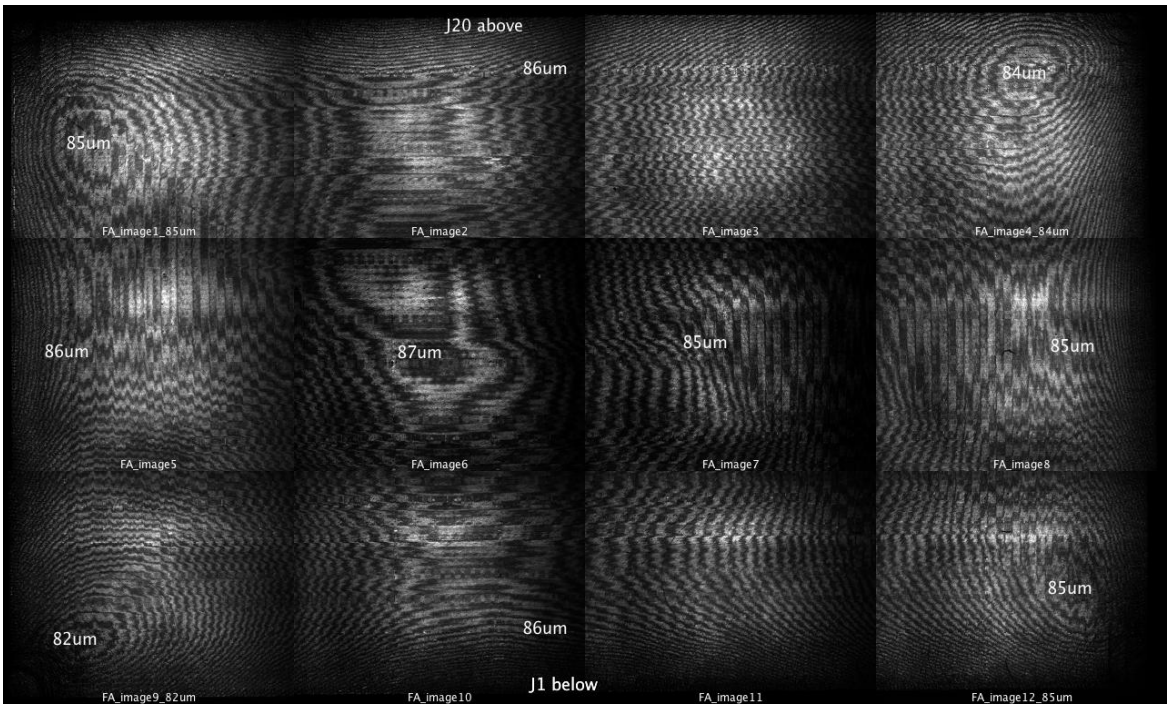

Figure 1: V7-585T DuTs after thinning & polishing.

For the March 2017 heavy ion test at TAMU, the thinning was performed by XRTC member JPL-NASA. Three V7-980T devices attached to their DUT carrier cards were thinned to less than 100 µm residual silicon substrate.The instrument used for this purpose was an Ultratec ASAP-1 milling machine, with no temp or curvature correction performed. Residual thickness measurements were conducted on two samples and the results are given in Fig. 2 for the thinner device. The device with s/n: 66603 is about 10 microns thicker than this device, and a cauldron-shape was achieved, where the thinnest region is located near the die center [13]. An overview over each V7-980T-DUT's die thickness is provided in Tab. 4

Table 4: Die thickness for each V7-980T DUT

	Die Thickness $[\mu m]$				
DUT s/n	min.	center	max.	avg.	std.dev.
66603	90.1	90.1	117.3	99.6	
66605	93.0	96.7	103.3	104.6	7.74
66607	80.4	80.6	103.3	87.5	

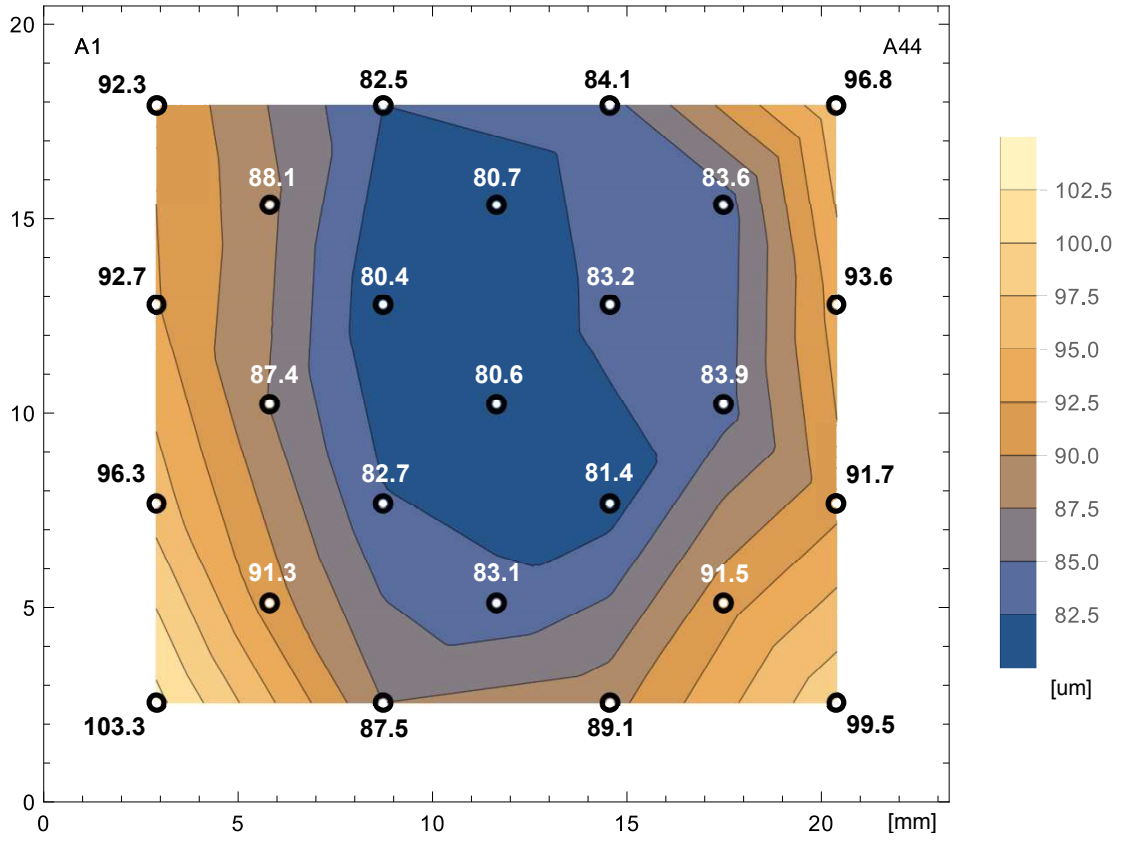

Figure 2: Contour plot of residual silicon thickness for DUT s/n:66607, interpolated from an array of 25 spot measurements using an IR laser system.

Variation in thickness represents a systematic error in LET, which is dependent on exactly where on the die the tested structures reside. Table 5 contains LET assignments obtained with the (SRIM-based) SEUSS modeling software [12], at three thickness levels as measured in Fig. 2.

Certain fabric-elements are arranged as column-like structures and spread across the whole die, e.g., CRAM and BRAM. The LET for such structures behaves as distribution with an average value approximated by the thickness value, and a spread indicated by min/max thickness. More localized structures sample less of the thickness variation, e.g., PLLs are located predominantly in the center (thinnest) region of the die [13]. This allows for tighter LET assignments for these structures.

In contrast, IOB tiles are located along the top and bottom edge of the die depicted in Figure 2. As these silicone regions are thicker, especially in the corner areas, LET assignments must be adjusted accordingly. For data obtained for IOBs, the higher-end arms of data error bars are more appropriate for these structures.

Table 5: LET Assignment $\left[\text{MeV cm}^2/\text{mg}\right]$

		Die Thickness $[\mu m]$		
Ion Species	**Angle**	80.4	95.1	110
^{14}N	0°	0.598	0.600	0.602
^{14}N	0°	1.10	1.10	1.10
^{20}Ne	0°	1.60	1.60	1.60
^{20}Ne	0°	3.00	3.00	3.00
^{40}Ar	0°	6.20	6.30	6.40
^{40}Ar	0°	10.2	10.7	11.4
^{40}Ar	50°	10.3	10.6	11.0
^{40}Ar	0°	15.6	18.0	17.0
^{40}Ar	65°	18.0	19.3	21.0
^{84}Kr	0°	23.1	23.8	24.5
^{84}Kr	50°	40.0	42.4	45.1
^{84}Kr	65°	79.1	91.6	54.0

9 CRAM-Cell Cross-section

In this characterization report, we utilize CRAM cell cross-section data of the Series-7 family as an aid to estimate bit-error rates. We obtain average number of critical CRAM bits affecting a particular design under test by comparing it to the CRAM-induced cross-section of a specific test design.

[Sebas]: Comment a paragraph on the AVF factor, and cite an appropriate reference. [CMF]: I don't see how this discussion makes sense here, at least considering the text that I have gone through up until now. Leaving this comment here with a TODO for future reference

The architecture of *Kintex-7* and *Virtex-7* CRAM cells is essentially identical. Hence, we characterize the *Series-7* CRAM-cell cross-section based on radiation-test data from both Kintex-7 and Virtex-7 devices. To do so, we can rely on per-bit CRAM cell upset cross-section data for *Kintex-7* devices obtained through static tests by XRTC member D. S. Lee *et. al.* [1].

As part of ongoing consortium research, a better fitting Weibul curve than the one report in [1] is possible considering the back then generated data. In Fig. 3, we depict CRAM-cell upset data with the original Weibul fit by D.S. Lee *et. al.* from [1], as well as an improved curve, denoted as XRTC 2018.The total squared error of the original fit curve was 8.22×10^{-18} with a correlation coefficient of 0.980, whereas the regenerated XRTC fit yields 1.24×10^{-18} total squared error and a correlation coefficient of 0.866.

Due to the better quality of the updated fit, we will therefore consider as *7-Series* inherent CRAM cell cross-section the regenerated recent XRTC Weibull curve fit as depicted below.

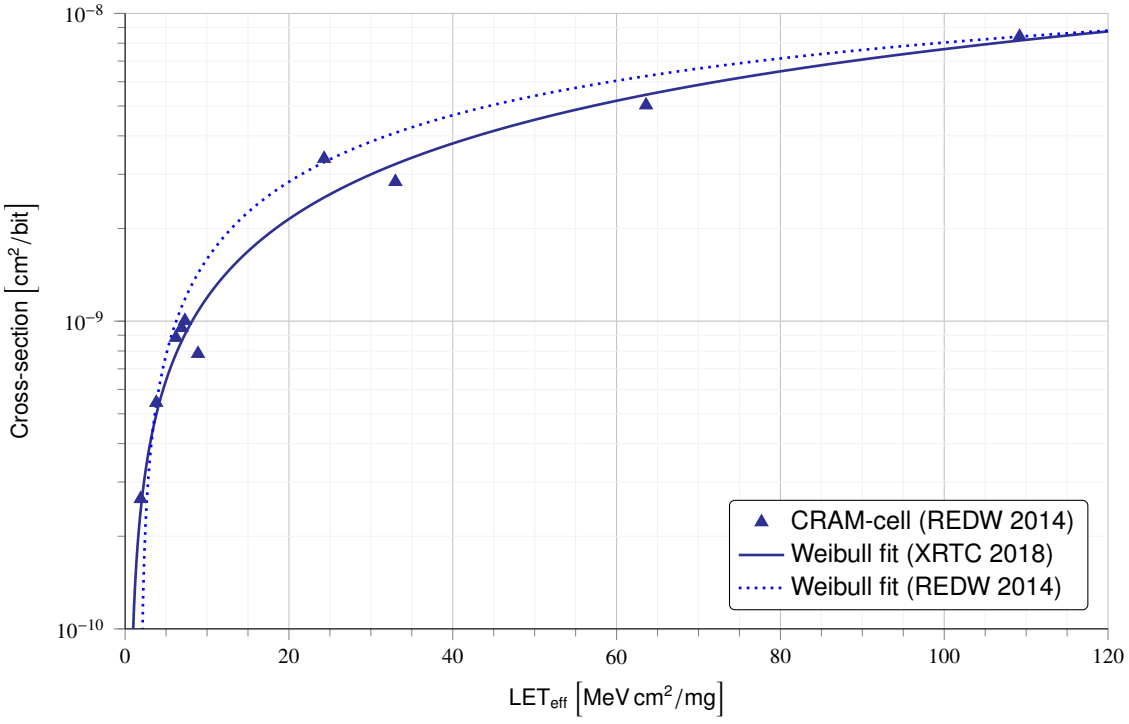

Figure 3: *7-Series* CRAM-cell upset cross-section, experimentally obtained by Lee *et. al.* [1] in heavy ions. Cross-section error bars are omitted, as they are smaller than the point data markers. For the Weibull curves, the associated parameters are: *(a) Current (XRTC 2018):* $\sigma_{sat} = 3.24 \times 10^{-8}$cm^2/bit, $L_{th} = 0.495$, $W = 474$, $S = 0.84$; *(b) Original (REDW 2014):* $\sigma_{sat} = 1.43 \times 10^{-8}$cm^2/bit, $L_{th} = 1.9$, $W = 125.3$, $S = 0.78$. The data points inherited from [1] Fig. 1

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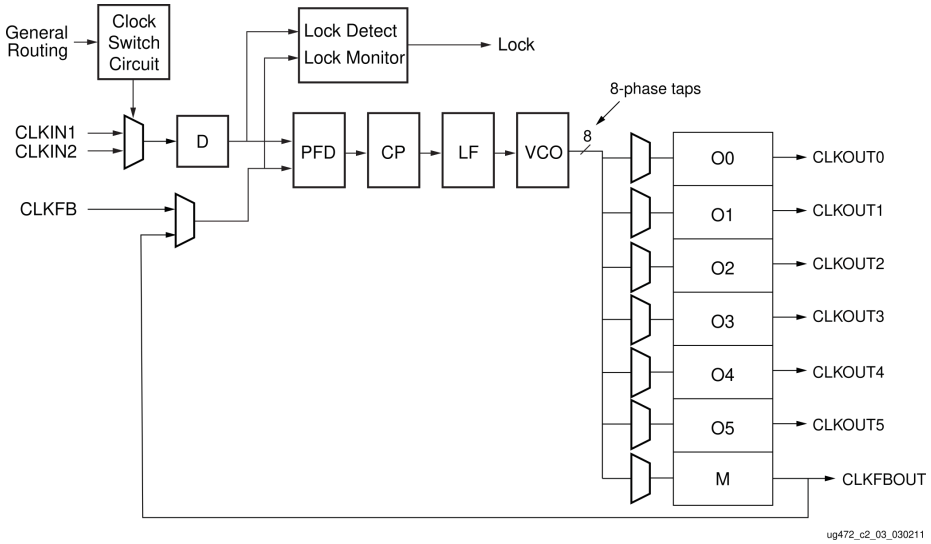
10 Clocking Resources (CMT) Test Results

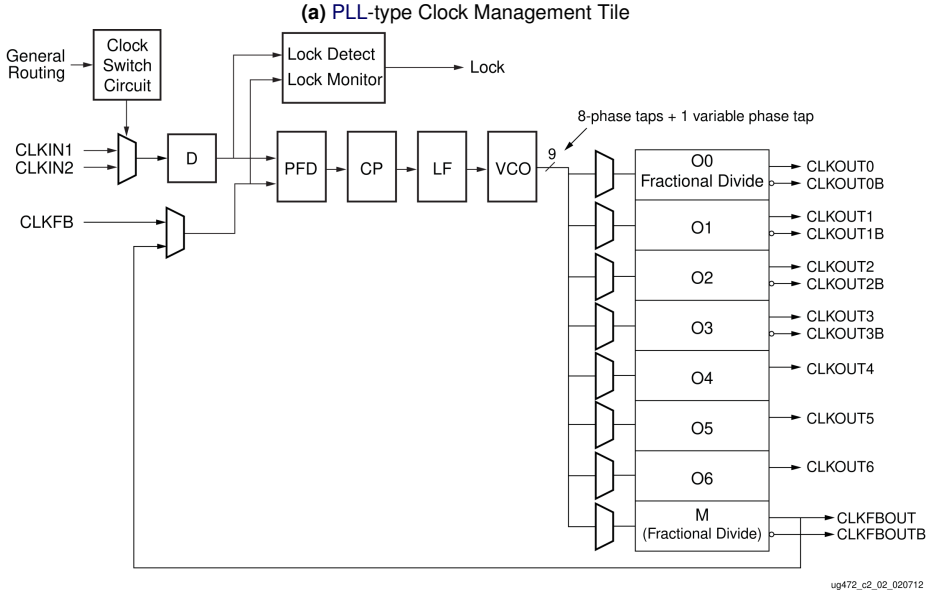
10.1 Introduction

The Clock Management Tiles (CMTs) in *Xilinx 7 Series* devices each consist of Mixed-Mode Clock Manager (MMCM) and Phase-Locked Loop (PLL) elements. CMTs are organized in vertical columns adjacent to the IOBs. They provide access to *vertical* global clock routes and *horizontal* regional clock routes, as shown in Figures 5 and 6.

The functionality offered by both the MMCM and PLL primitives are frequency synthesis, phase shift and de-skew, as well as jitter filtering. A PLL offers a subset of the functionality of an MMCM primitive, with differences being described in detail in the *7 Series FPGAs Clocking Resources User Guide*, UG472 [14]. Hence, differences in SEE test results between MMCMs and PLLs are to be expected due to differences in programmability as well as fundamental implementation. Complete details of the CMT functions and clock routing resources are documented in the [14].



(a) PLL-type Clock Management Tile



(b) MMCM-type Clock Management Tile

Figure 4: The tested CMT primitives. Among others, main differences include support for differential output clocks and phase shifting capability for MMCM-type CMTs.

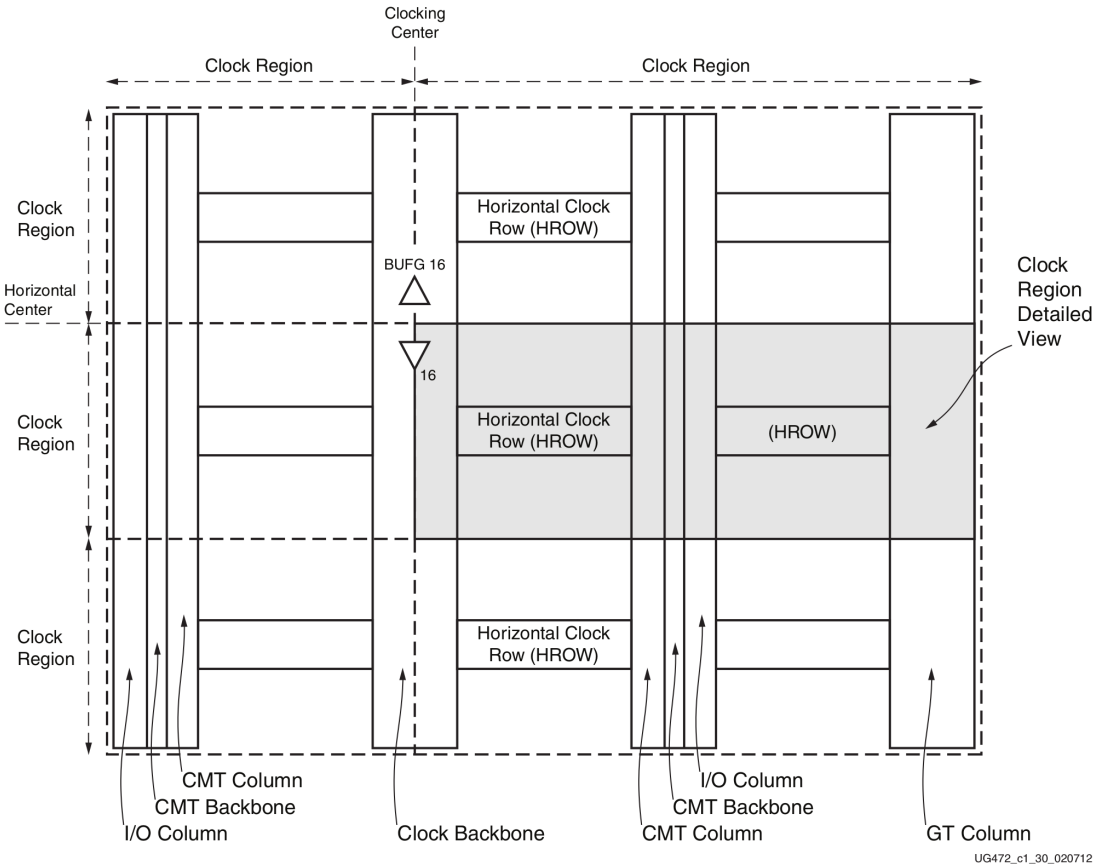


Figure 5: 7 Series FPGA high-level clock architecture view.

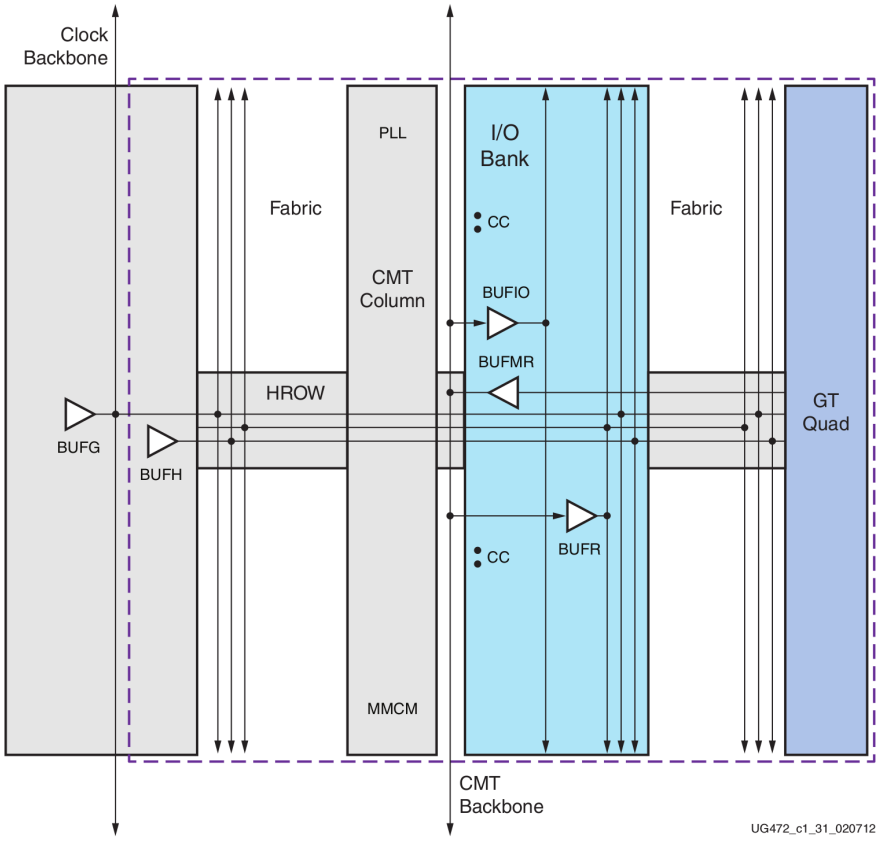


Figure 6: Basic view of a clock region.

10.2 Test Methodology and IP

For conducting the *Virtex-7* SEE clocking test, we leveraged the V-5QV heritage DUT design, originally conceived and implemented by George Madias of Boeing. A basic block diagram of the DUT test design is shown in Figure 7. The overall DUT design contains two instances of a clock monitoring and validation setup, depicted in Figure 7 as test instance #1 and #2.

Each test instance contains a primary and secondary clocking source, both using either an MMCM or PLL primitive. These two MMCM or PLL clock primitives operate in parallel and independently monitored for upsets. The input clocks are frequency-multiplied by a factor of 2 by the respective MMCM/PLL primitive.

The MMCM/PLL clock outputs are checked within each instance of the DUT independently by the indicated validation circuitry IP. The validation circuitry IP is radiation-hardened by design through the use of triple-modular redundancy (TMR). If the primary CMT is upset, the validation circuitry switch to the secondary CMT instance and resets the upset primary CMT. The validation circuit switch back to the primary clock if it detects a upset in the secondary CMT element which it currently monitors. For transients inducing effects with an extended duration (Intermittent faults), switching and resetting of primary/secondary CMTs may repeat multiple times until the circuit has stabilized again. Besides the CMT primitive instantiated, the DUT design used in MMCM and PLL tests were identical.

As depicted in Figure 7, three external clocks are brought into the DUT and attached to the test design's clock sources. The first and second external clock from Bank 11 are attached to the first and second CMT in both test instances. The third external clock from Bank 37 is attached only to the validation and control circuitry in both instances.

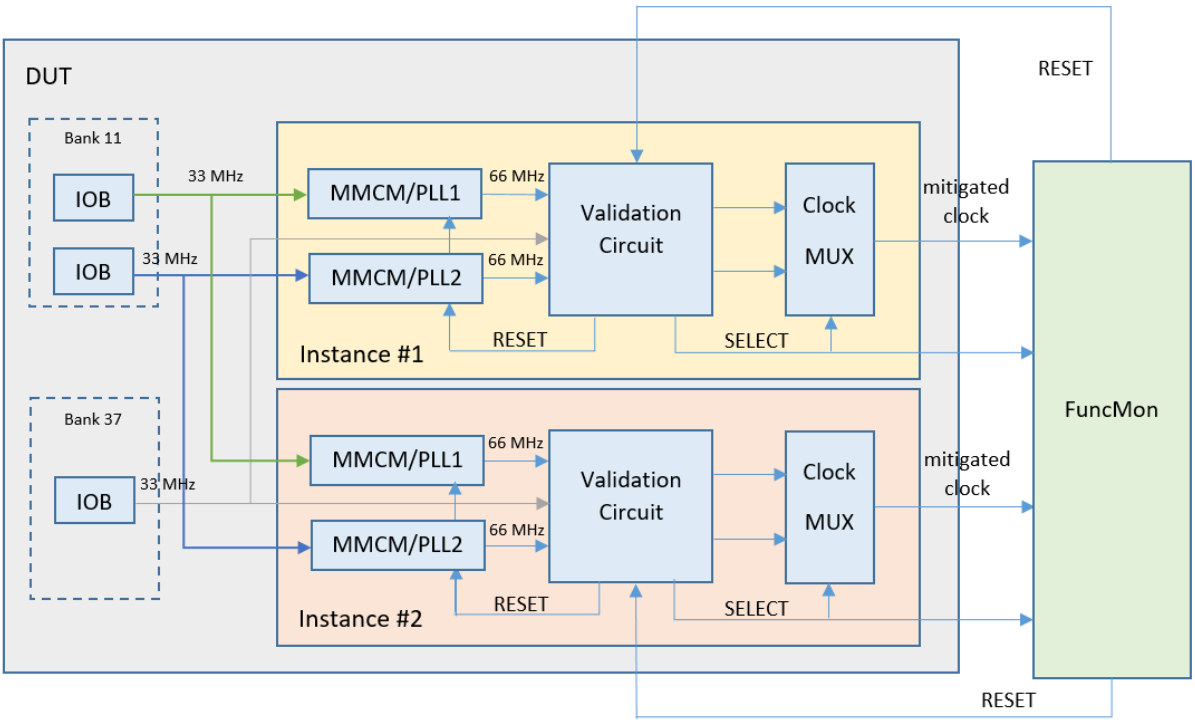


Figure 7: The DUT design utilized for CMT characterization.

The FuncMon observes the mitigated clock output from each instance. The FuncMon design used for both types of clock tests was identical.

After 6.7 seconds, the total duration of a scrubbing cycle, sufficient time has passed for events caused by a configuration upset to be scrubbed by ConfigMon. When a clock output from either instance stops for 10 seconds, FuncMon and the validation circuit are externally reset, and FuncMon records a global outage event. Therefore external intervention would be required to reset the DUT after 10 seconds. We consider such a

condition as SEFI-like events. No such SEFI-like clock outages were observed, and all events were resolved by the test setup reset autonomously. No full setup resets or intervention to reconfigure DUT or FuncMon were required to recover an upset clock source.

The upset mitigation scheme implemented within this test design generates three distinct error signatures that are observable by FuncMon:

- *single clock upset* – a clock outage with a duration < 100 ms by an upset to the primary CMT. The DUT's validation circuitry in each instance can successfully mitigate such events by switching from the current primary clock source to the secondary source;
- *instance outage* – clock outages with a duration > 100 ms caused by upsets effecting **both** the primary and secondary **clocks** of **a single test instance**. The validation circuitry of an instance can not mitigate this failure mode, but the DUT continues to provide a correct clock source through the other test instance in the DUT design. Correct operation of the affected test instance resumes once at least one CMT of the two CMTs in the affected instance becomes functional again;
- *global outage* – outages with a duration > 100 ms effecting **both clocks** of **both test instances** simultaneously (all clocks). This failure signature is resolved by either autonomously by the validation circuit when at least one clock recovers, or due to external intervention, e.g., a reset from FuncMon or ConfigMon.

10.3 Results: Measured Cross Sections

The MMCM and PLL cross sections for the three different error signatures are shown in Figures 8 and 9, respectively. The cross sections are measured as a function of LET.

Error signatures can be correlated with faults occurring in specific fabric regions in some aspects. An instance-wide clock outage is the result of a particle interacting with fabric-infrastructure or logic shared by both the primary and secondary clock sources. A global clock outage is the result of a particle interacting with fabric-infrastructure or logic shared by all clock sources or instances under test.

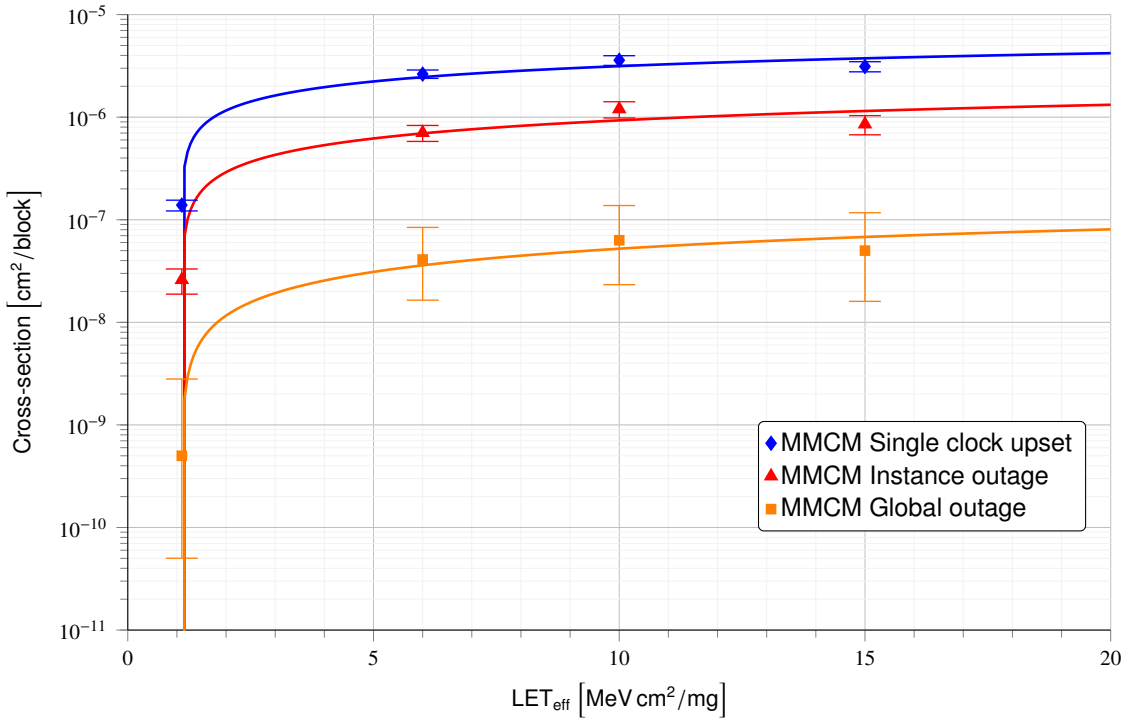


Figure 8: Cross-sections of *Virtex-7* MMCM clock resource glitches caused by heavy ions. Weibull fit parameters are: *(a) Single:* $\sigma_{sat} = 1.00 \times 10^{-5}$, $L_{th} = 1.09$, $W = 65.0$, $S = 0.49$; *(b) Instance:* $\sigma_{sat} = 4.00 \times 10^{-6}$, $L_{th} = 1.09$, $W = 99.7$, $S = 0.55$; *(c) Global:* $\sigma_{sat} = 2.00 \times 10^{-7}$, $L_{th} = 1.09$, $W = 48.0$, $S = 0.71$.

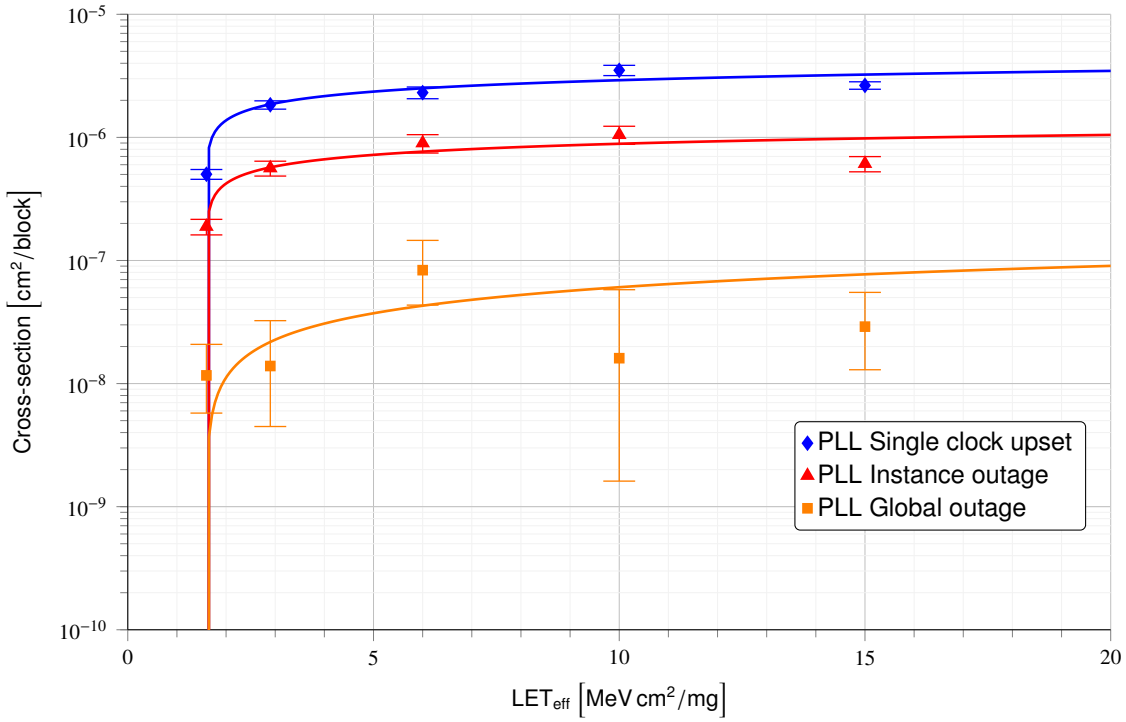


Figure 9: Cross-sections of *Virtex-7* PLL clock resource glitches caused by heavy ions. Weibull fit parameters are: *(a) Single:* $\sigma_{sat} = 8.00 \times 10^{-6}$, $L_{th} = 1.59$, $W = 129$, $S = 0.29$; *(b) Instance:* $\sigma_{sat} = 2.00 \times 10^{-6}$, $L_{th} = 1.59$, $W = 49.8$, $S = 0.30$; *(c) Global:* $\sigma_{sat} = 3.00 \times 10^{-7}$, $L_{th} = 1.59$, $W = 105$, $S = 0.59$.

Since the clock sources under test for both instances both come from I/O bank 11, an upset to that I/O bank would cause a clock global outage observed by the validation circuitry. In contrast, a hit on single IOB primitive would manifest in a single clock upset observed by both test instances. We can compare the computed CMT cross sections to that of the IOBs in Section §11 to validate this hypothesis.

For the MMCM/PLL single clock upset and instance outage signatures, the cross section for an individual LVCMOS18 or LVDS IOB upset is on average 2-3 orders of magnitude lower than for CMTs. The I/O circuitry thus has a minimal effect on clocking upsets in these two upset signature types. This means that the reported cross sections are representative of the MMCM/PLL blocks, clock routing, and configuration bits associated with the clocking structure.

For global upsets and I/O bank upsets, the CMT and IOB Weibull fits are very similar. Hence, we can assume the majority of global upsets observed are due to particle events affecting entire I/O banks. Consequentially, the actual, true CMT cross-section representing global clocking events is much lower than that calculated in Figures 8 and 9.

Table 6 shows GEO-orbit upset rates computed with `CREME96`. For each CMT primitive and error signature, we express units as events/day/resource-instance. The measured cross sections and resultant GEO rates for PLLs and MMCM primtives are very similar. This is in line with data obtained during V-5QV testing. Figures 10, 11, and 12 show MMCM and PLL results superimposed for the three different error signatures.

Table 6: GEO-orbit Upset Rates

Signature	Nominal	Worst-Case
MMCM *Single*	1.75×10^{-4}	1.89×10^{-4}
MMCM *Instance*	4.53×10^{-5}	4.95×10^{-4}
MMCM *Global*	3.71×10^{-6}	4.11×10^{-6}
PLL *Single*	1.51×10^{-4}	1.65×10^{-4}
PLL *Instance*	4.63×10^{-5}	5.06×10^{-5}
PLL *Global*	1.86×10^{-6}	2.13×10^{-6}

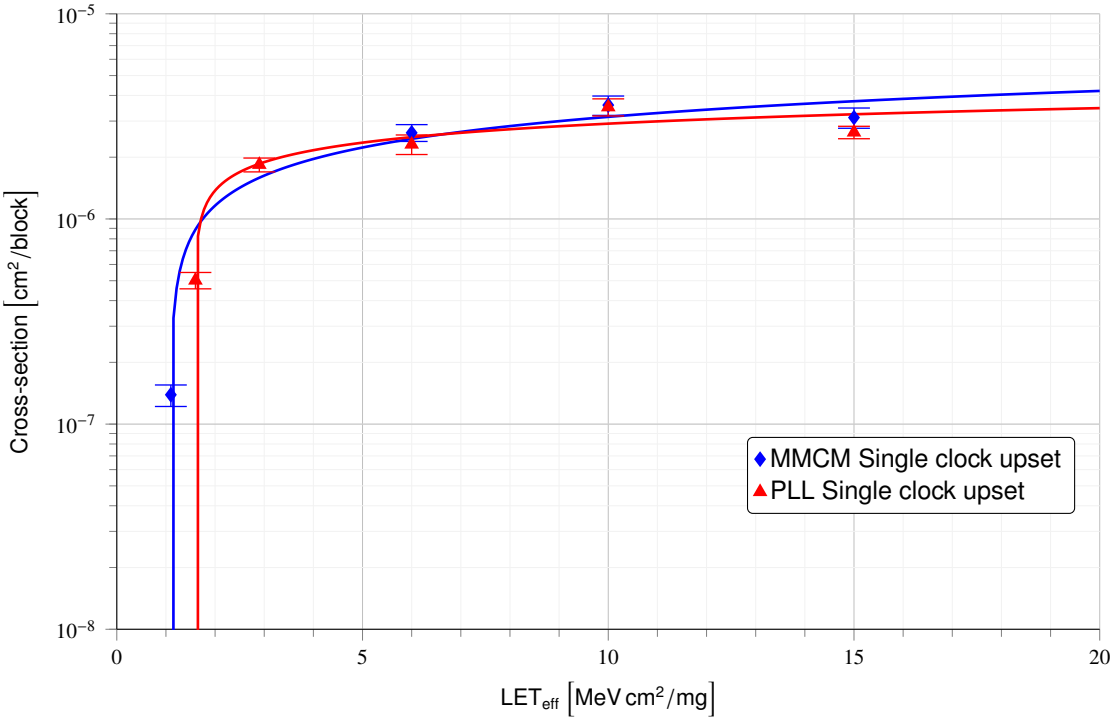


Figure 10: *Virtex-7* MMCM vs. PLL single clock upsets.

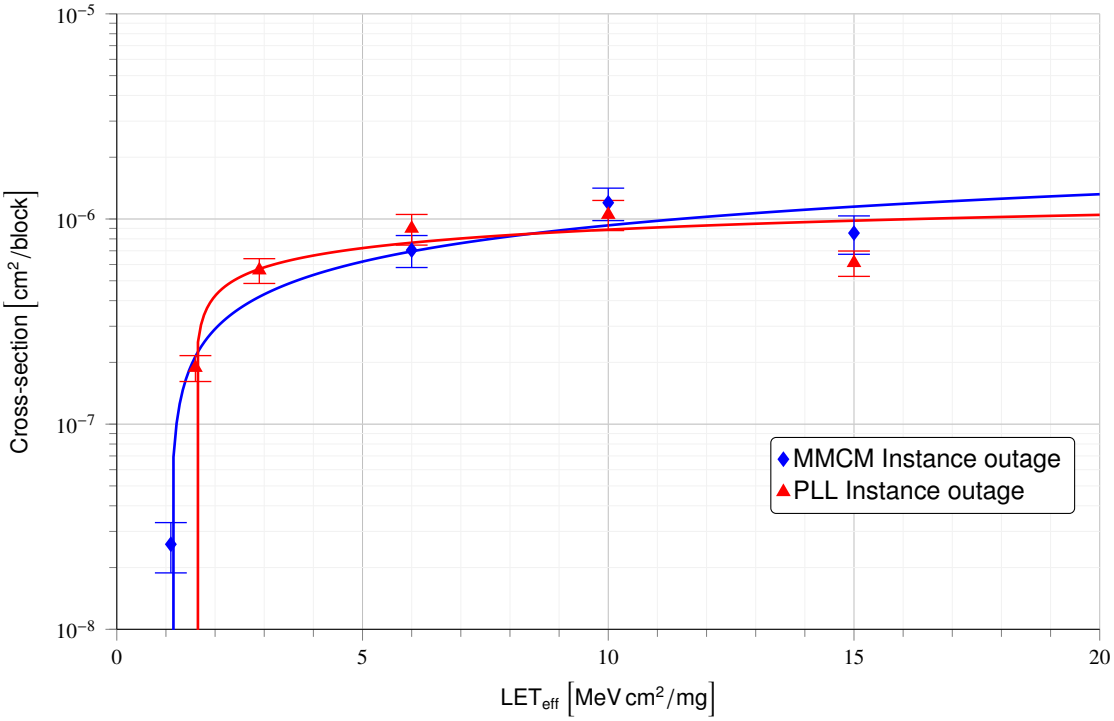


Figure 11: *Virtex-7* MMCM vs. PLL instance outages.

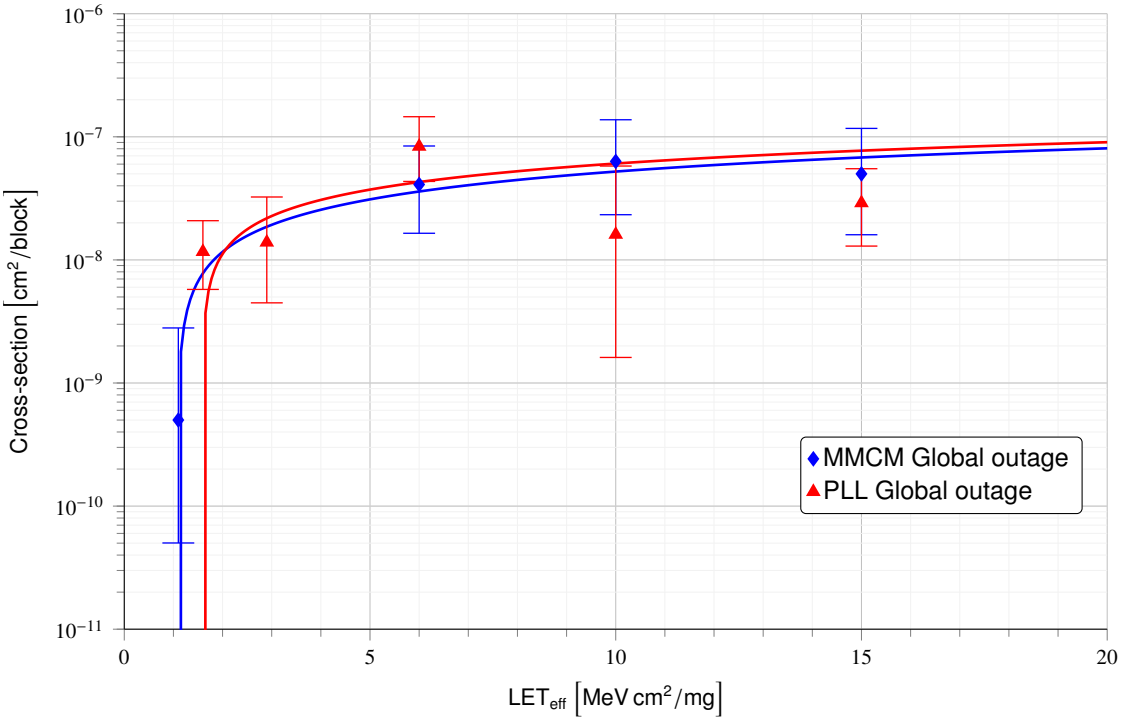


Figure 12: *Virtex-7* MMCM vs. PLL global outages.

10.4 Comparison to Virtex-5QV

In principle, single clock upsets should occur most frequently, followed next by instance outages, and lastly by global outages being the least frequent. We found this prediction to be true in the *Virtex-7* analysis reported here. However, this is not the case for the results reported in the *Virtex-5QV* Architectural Features SEU Characterization Summary. Further data analysis performed for the *Virtex-7* XRTC SEE test campaign, and a review of archived *Virtex-5QV* test data was conducted. This analysis indicates inconsistencies in the original *Virtex-5QV* clocking data analysis.

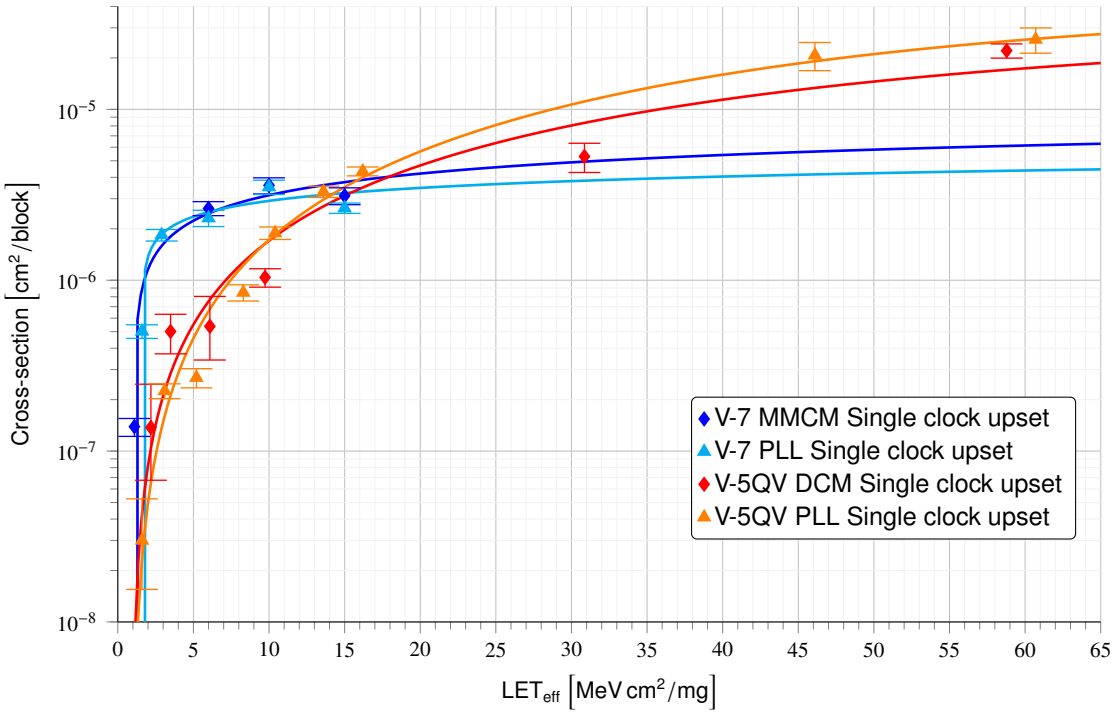


Figure 13: *Virtex-7 vs. Virtex-5QV* single clock upsets. Weibull fit parameters for V-5QV data, are:
(a) DCM: $\sigma_{sat} = 3.00 \times 10^{-5}$, $L_{th} = 0.91$, $W = 65.3$, $S = 1.44$; *(b) PLL:* $\sigma_{sat} = 4.00 \times 10^{-5}$, $L_{th} = 0.91$, $W = 58.4$, $S = 1.68$.

The V-5QV cross sections reported for the different error signatures are exactly inverse to what would be considered logical. In the V-5QV report, global clock upsets had the largest cross-section and single clock upsets had the smallest. Hence, we re-analyzed the raw V-5QV data using the (improved) *Virtex-7* analysis pipeline. This produced results more in line with our expectations. Upon comparing the V-7 data results to the V-5QV data and result set, our conclusion is that the V-5QV results presented in the Architectural Features report are flawed.

An errata showing the new V-5QV results using the V-7 analysis algorithm pipeline has been published to the Xilinx Space Lounge. The original V-5QV data analysis was not revisited to thoroughly identify the source of the errors in the Architectural Features report. However, the errata contains results of running both raw data sets through the latest XRTC CMT analysis algorithm pipeline, which provides the most accurate comparison also presented here. A comparison of the *Virtex-5QV* and *Virtex-7* single clock upsets is shown in Figure 13.

There is one significant difference in the selection of I/O pins used for the clock inputs between the *Virtex-7* and *Virtex-5QV* DUT designs. In the original design of a test instance used during *Virtex-5QV* tests, a single external clocks drives both clock primitives as well as the validation circuitry. Each instance is driven by an independent external clock delivered from a separate I/O bank. The V-5QV design is depicted in Figure 15. In the new test instance design used during *Virtex-7* tests, both CMTs are driven by separate clock sources. The first CMT in each instance is driven by one clock source, and the second CMT in each instance is driven by a second source. Both clocks sources were obtained from IO Bank 11. Furthermore, the validation circuitry in the V7 design has a dedicated clock source obtained from IO Bank 37.

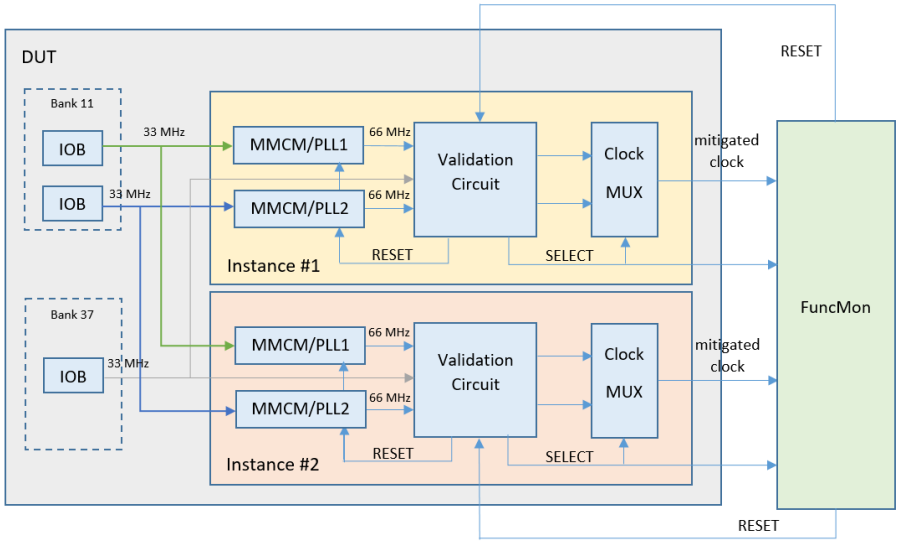


Figure 14: The V-7 CMT DUT design.

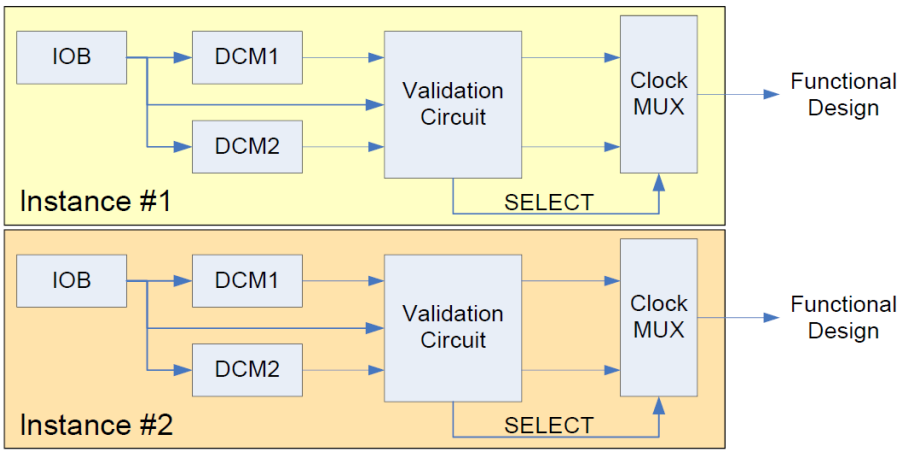


Figure 15: The V-5QV CMT DUT design.

The different clocking setup has little direct impact on the actual data produced. However, it does have an impact on how instance and global outage results from the V5-QV and V7 testing are to be correlated. On the *Virtex-5QV* DUT, an I/O bank hit would manifest in an instance outage. In contrast, the same upset would no longer cause an instance outage but a global outage in the *Virtex-7* DUT. Therefore it would be more accurate to compare *Virtex-7* global outages to *Virtex-5QV* instance outages. This comparison is depicted in Figure 16. As can be seen, the depicted curves are similar in shape to the single clock upset comparison.

Only a single DCM instance on V-5QV outage was observed when re-analyzing the raw test data obtained back then with updated analysis algorithm pipeline. Therefore we are unable to obtain a Weibull fit for V-5QV DCM outages. However, the single DCM data point matches the PLL curve. The updated analysis algorithm pipeline did not find any global outages in the V-5QV data.

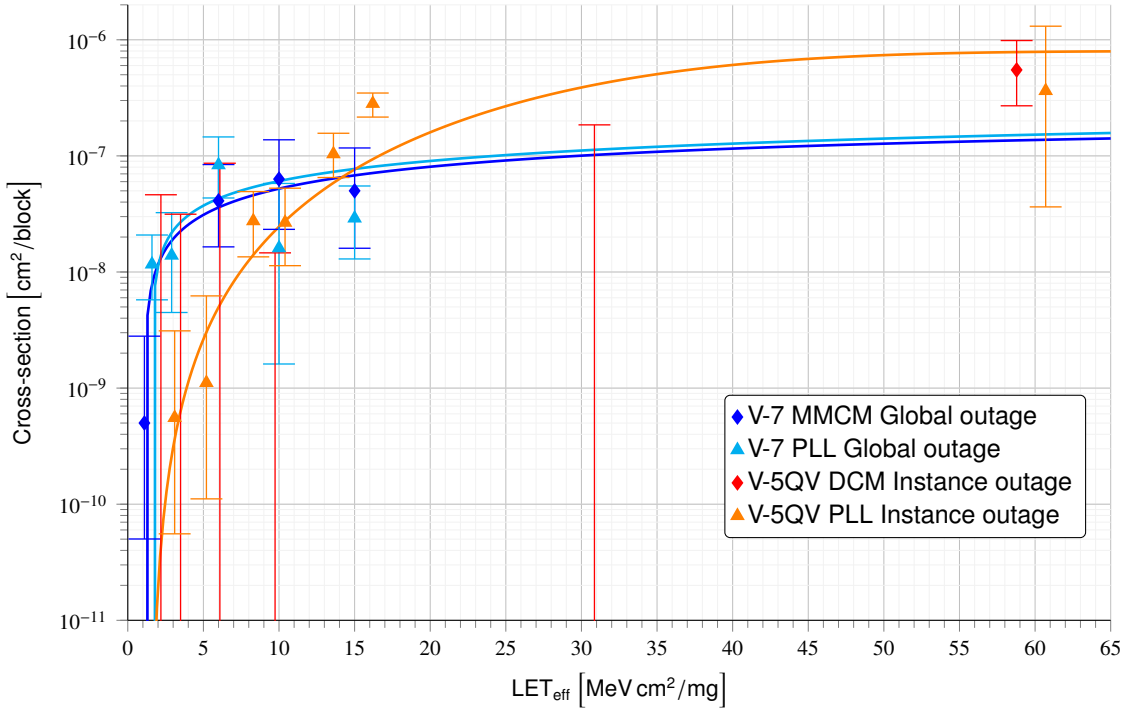


Figure 16: *Virtex-7* global outages *vs.* *Virtex-5QV* instance outages. Weibull fit parameters for V-5QV PLL data, are: $\sigma_{sat} = 8.00 \times 10^{-7}$, $L_{th} = 1.50$, $W = 33.5$, $S = 2.53$.

10.5 Remarks for Future Tests

Further improvements to the original test methodology should be explored for the KU060 test campaign in order to provide better visibility. In general, the V-5QV clocking scheme depicted in Figure 15 should be used instead of the one used in the V-7 test runs 14.

10.6 Summary

The *Virtex-5QV* CMT DUT design was migrated to *Virtex-7* technology and used to gather valuable single event effect data on the *7 Series* PLL and MMCM design primitives. The clock input connections were modified from the original design, which leads to differences in the correlation of the results between V-5QV and V-7. Note that the susceptibility of the clock tree distribution is not included. The analysis presented here provides accurate cross-section data on the *Virtex-7* Clocking Management Tiles that can be used to predict realistic orbit rates and error signatures.

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11 Input/Output Blocks (IOB) Test Results

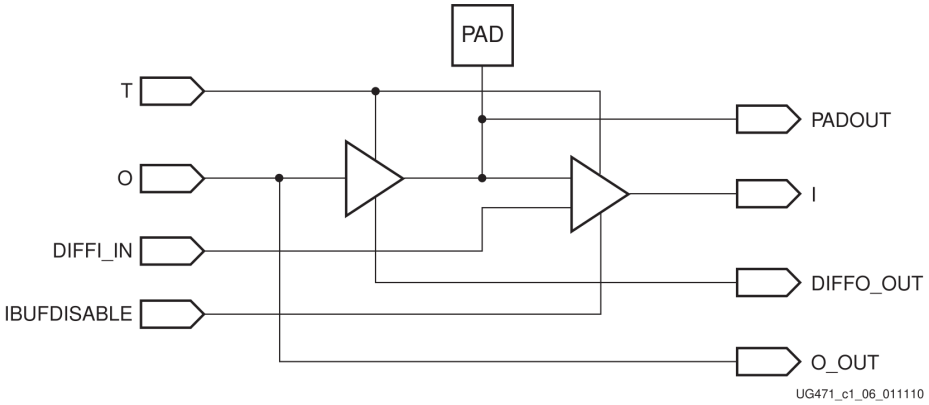
Analysis by Sebastián E. García, Slabs, Buenos Aires, Argentina –

11.1 Introduction

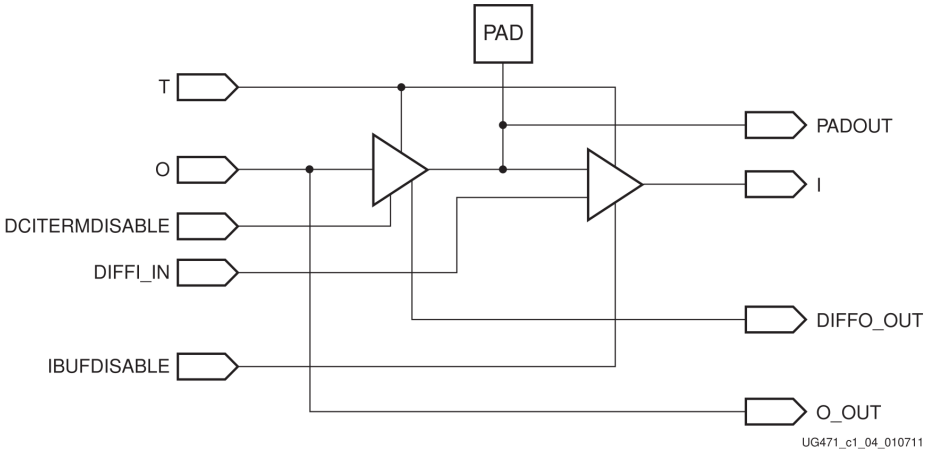
The Input-Output Block (IOB)-design used in Series-7 FPGAs include several changes and improvements as compared to earlier FPGA generations. These are described in detail in [15]. Series-7 FPGA IOB that are designer usable are either part of a high-range (HR) or high-performance (HP) bank. The layout of IOBs in HR and HP banks is depicted in Fig. 17.

I/O tiles exist in two forms: as single and differential-capable IOBs. Each single ended IOB can be configured as either LVCMOS, LVTTL, HSTL, PCI, or SSTL. A differential IOB can be configured as either LVDS, Mini LVDS, RSDS, PPDS, BLVDS or differential HSTL/SSTL. Naturally, this abundance of configuration modes available makes exhaustive testing of all these modes unfeasible.

As most of these configuration modes utilize very similar or even identical logic to realize the relevant functionality, doing so is also unnecessary. Considering knowledge obtained during V-5QV characterization, the tests for the Virtex-7 FPGA family were limited to the following interface configurations: LVCMOS, LVDS, and HSTL. Furthermore, the XRTC had originally planned to also carry out testing for IDELAY/ODELAY with IOB resources. However, this test went unfilled due to cancellation of the third heavy ion radiation test. This was deemed acceptable at that time. However, in consequence only a limited amount of valid IOB test data had been generated overall.



(a) A differential HR IOB.



(b) A differential HP IOB.

Figure 17: Block Diagram of differential-capable Series-7 High-Range and High-Performance I/O Tiles. Tiles exist either regular (differential) or single-ended. Single-ended IOBs do not implement DIFFO_OUT and O_OUT signals but are otherwise essentially equivalent [15].

The V7-585T FPGAs used in the first heavy ion radiation test of the XRTC Series-7 test campaign offers both HR and HP banks. However, as depicted in Figure 18, most larger V7 family devices are exclusively outfitted with HP-type banks. This includes the including the V7-980T DUT. Hence, testing was conducted with HP-IOBs on all V7 devices to assure comparable results are obtained.

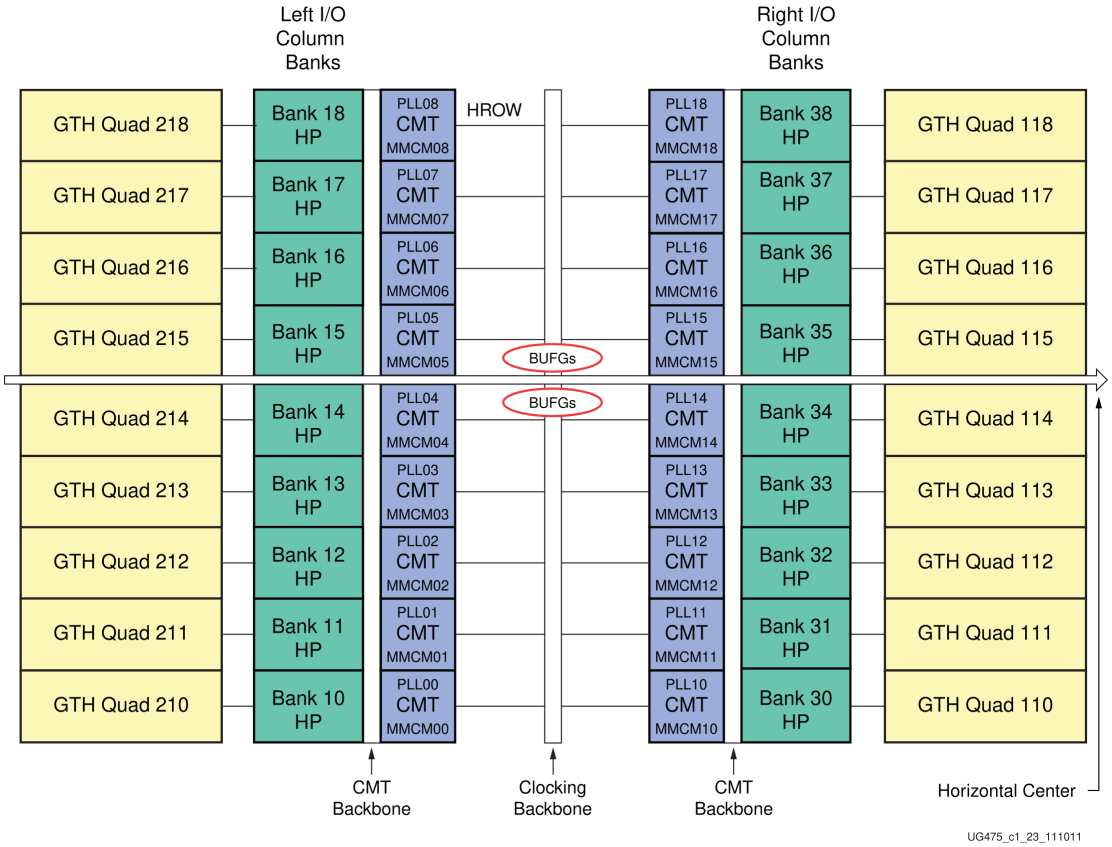


Figure 18: 7 Series FPGA I/O-bank layout.

11.2 Test Methodology and IP

IOBs were tested at 1.8 Volts in the following interface configurations LVCMOS, LVDS, and HSTL. The optional input and output SERDES register was tested with LVCMOS-IOBs configured.

The test setup is a short 'loopback' of one DUT input excited by *FuncMon*, to a group of several DUT outputs monitored by the same *FuncMon* FPGA. Individual output upsets are clear while group upsets indicate an input hit. Due to practical constraints, for some test cases this input-output relation is 1:1 (*i.e.,* a given input simply routed to one output), meaning that for these cases we are unable to discriminate between input or output events. As with the *Virtex-5QV*, the *Virtex-7* shows three upset modes in addition to relevant configuration upsets (that affect IOB functionality until scrubbed): **1)** data transients, **2)** individual bank outages, and **3)** global I/O outages.

Regarding cross-sections computed for upsets on individual inputs or outputs, for all the tested IOB standards, the *per-resource cross-section* term refers to a given cross-section normalized to the total number of inputs or outputs under test. Also, in this context of IOB testing, the term *low-frequency* corresponds to a test running with 2 MHz signals, whereas *high-frequency* corresponds to the use of 33 MHz signals.

11.3 Results: Individual LVCMOS-IOBs

For the LVCMOS18 (LVCMOS@1.8 V) IOB block standard, three test variants were in-beam tested; these can be labeled as: **a) LVCMOS-UL:** Unregistered and Low-frequency, **b) LVCMOS-UH:** Unregistered and High-frequency, and **c) LVCMOS-RL:** Registered and Low-frequency.

The result of the LVCMOS-UL test variant is shown as cross-section discrete points in Fig. 19, for both inputs and outputs. For these transient upsets, we see there are not enough valid experimental data points available to properly fit a Weibull curve. For comparison purposes, experimental results for CRAM-induced upsets affecting the LVCMOS-UL test are also shown in Fig. 19. Additionally, here we recall the Weibull fit generated in Section §9 for the *7-Series* inherent CRAM cell upset (per-bit) cross-section measured in the early work of D. S. Lee *et. al.* [1]. For each set of our (LVCMOS-UL) input and output CRAM-induced upset experimental points, we can scale that cross-section (§9) with an integer number, in order to achieve an appropriate "inspection fit" with the plotted data points. This is shown as two curves in Fig. 19, corresponding to scaling factors $N_I = 17$ and $N_O = 11$ for inputs and outputs, respectively. Note that these integers represent the average number of critical bits involved in this particular IOB test setup, effectively affecting an IOB block[†].

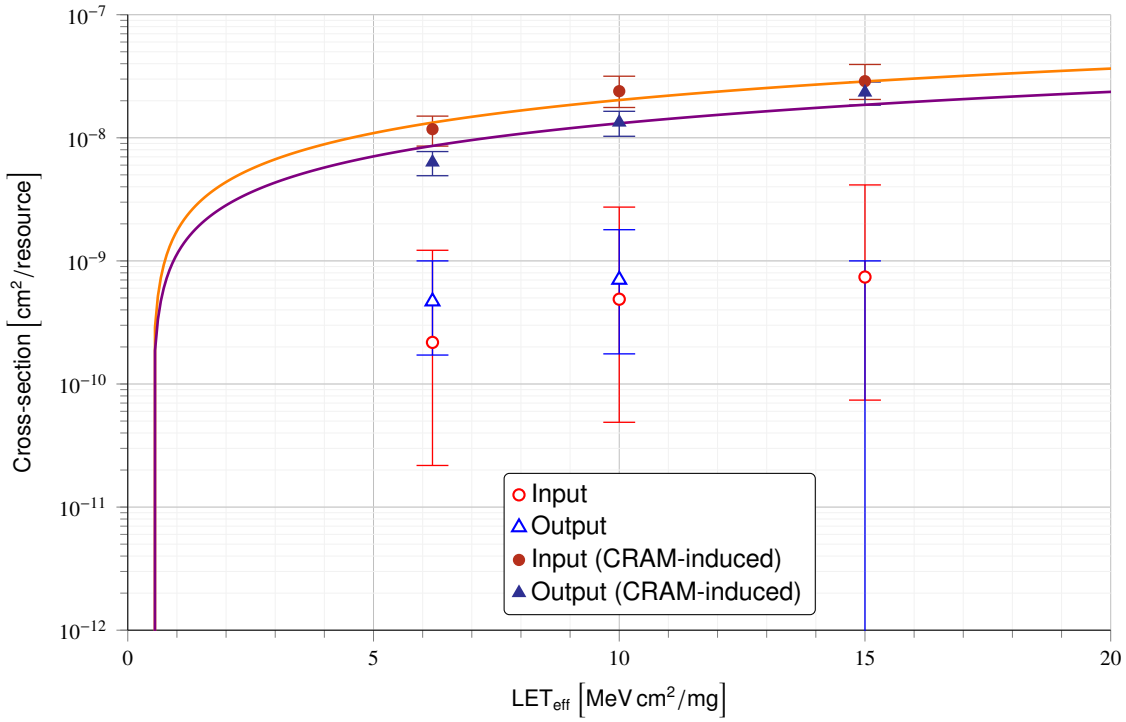


Figure 19: *Virtex-7* LVCMOS, transient upsets for *un-registered and low-frequency (UL)* test variant. For comparison, CRAM-induced upset experimental points are shown. The curves correspond to an integer scaling of the per-bit cross-section Weibull fit for CRAM cell upsets, as determined in Section §9 from the data of Lee *et. al.* [1]. The scaling factor for the upper curve is $N_I = 17$, while for the lower one we have $N_O = 11$.

For the LVCMOS-UH test variant, the result is shown as cross-section points in Fig. 20, for both inputs and outputs. Again, we see that there are not enough valid experimental data points available to properly fit a Weibull curve. Figure 20 includes both the experimentally-obtained points for CRAM-induced upsets (affecting this particular test), as well as the same CRAM cell cross-section "inspection fit" curves of Fig. 19. The overlapping error bars for the CRAM-induced upsets support the hypothesis that there's actually a single integer $N = N_I = N_O \simeq 14$ representing the average number of critical CRAM bits impacting this IOB test.

Figure 21 shows the result of the last test variant, LVCMOS-RL, as cross-section experimental points for both inputs and outputs. Here we have the largest amount of valid experimental data, and corresponding Weibull fits are shown. **[TBC]: Check the Input (transients, RL) Weibull fit.** Open red points are either: almost on the red curve, or above the red curve. (I'd expect the curve being more "centered" about the points). Sebas. As in the previous plots, Fig. 21 includes the points for CRAM-induced upsets affecting this particular test, and the same CRAM cell cross-section "inspection fit" curves of Fig. 19.

Next, we consider LVCMOS inputs' cross-sections, for all three test variants combined. In Fig. 22 we plot, for these combined inputs, transient and CRAM-induced upsets. Figure 22 also shows, for comparison purposes,

[†] Of course, on any real application HDL design, the average number of critical bits affecting an IOB will be larger, in general.

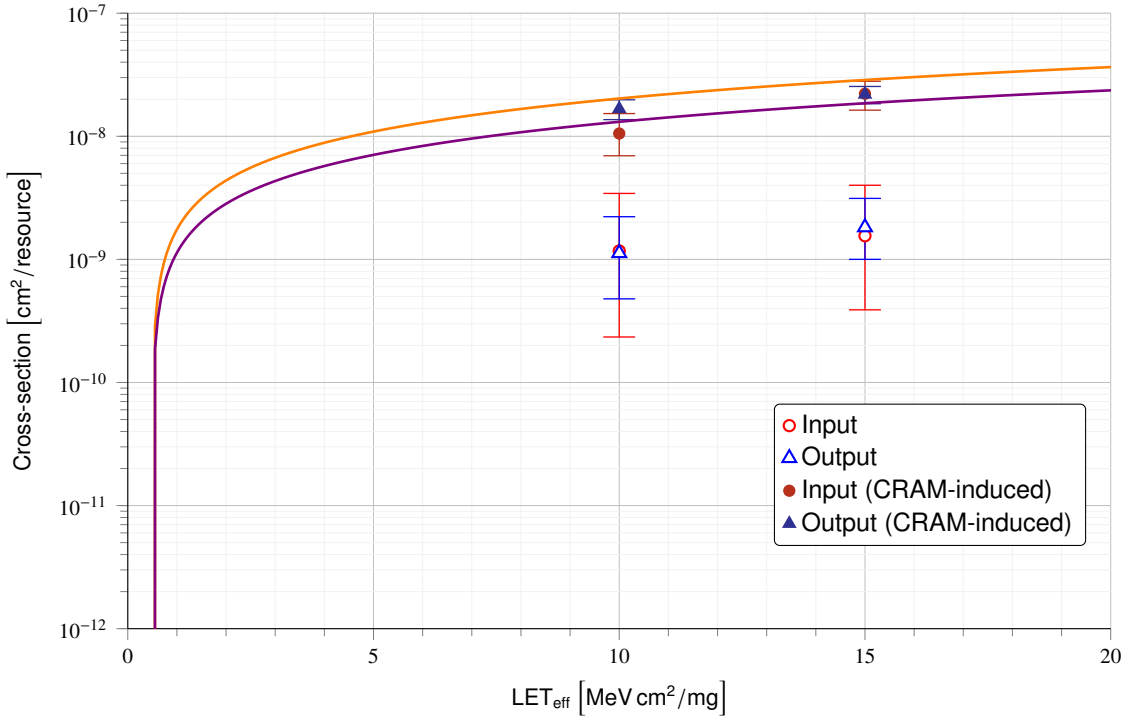


Figure 20: *Virtex-7* LVCMOS, transient upsets for *un-registered and high-frequency (UH)* test variant. Also, CRAM-induced upset experimental points are shown, together with the curves of the "inspection fit" from the CRAM cell cross-section (same as in Fig. 19).

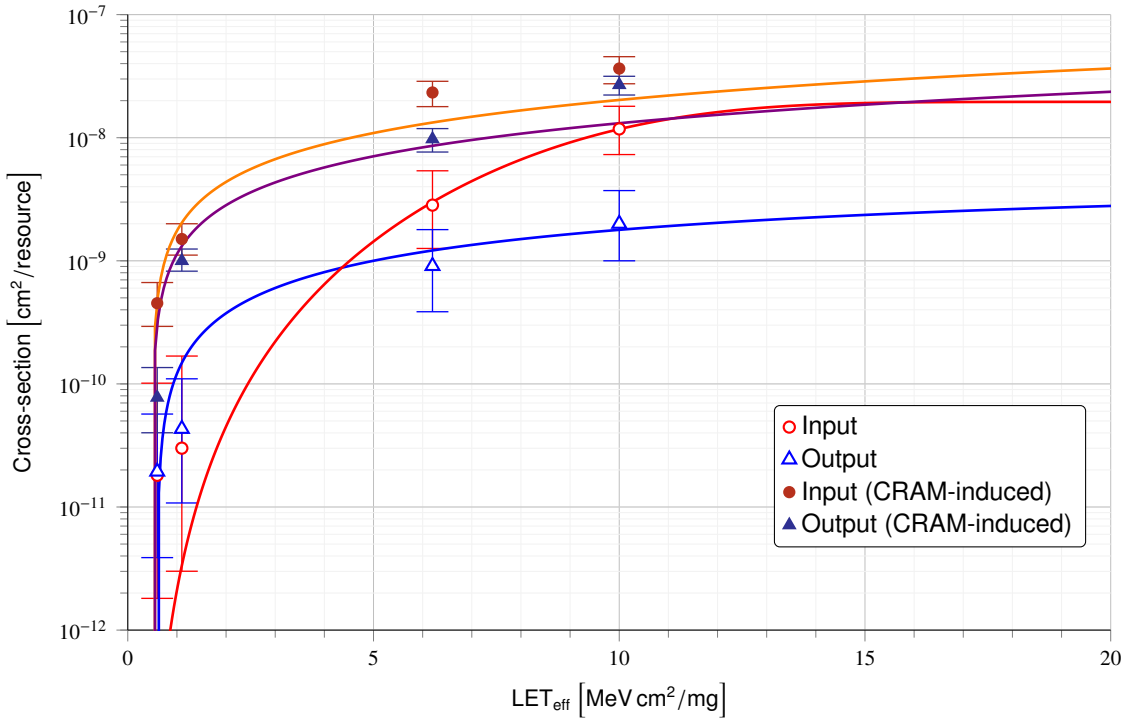


Figure 21: *Virtex-7* LVCMOS, transient upsets for *registered and low-frequency (RL)* test variant. For the corresponding Weibull fit curves, the associated parameters are: *(a) Output:* $\sigma_{sat} = 4.22 \times 10^{-9}$, $L_{th} = 0.595$, $W = 17.8$, $S = 0.934$; *(b) Input:* $\sigma_{sat} = 1.96 \times 10^{-8}$, $L_{th} = 0.308$, $W = 9.94$, $S = 3.43$. Also, CRAM-induced upset experimental points are shown, together with the curves of the "inspection fit" from the CRAM cell cross-section (same as in Fig. 19).

the Weibull fit resulting from registered input transient upsets on *Virtex-5QV* [11] . It's interesting to note that the cross-section due to CRAM-induced upsets on LVCMOS inputs are on the same order of magnitude of the cross-section due to transients affecting registered LVCMOS inputs on *Virtex-5QV*. We recall that, in the latter architecture, the cross-section for upsets on registered inputs are two orders of magnitude higher than un-registered ones, dominating the cross-section for combined inputs. **[TBC]:** This is, assuming the Weibull parameters on V-5QV AF report are correct. Sebas.

[TBC]: For V-5QV curves, here we are using Weibull parameters from AF Report, into the **INcorrect** Weibull equation (Gary, please note this curve is still appreciably different from Fig.8b (blue) in the V-5QV AF manual. . .). **Still pending: Correction of the Weibull flaw in the V-5QV AF report.** Sebas.

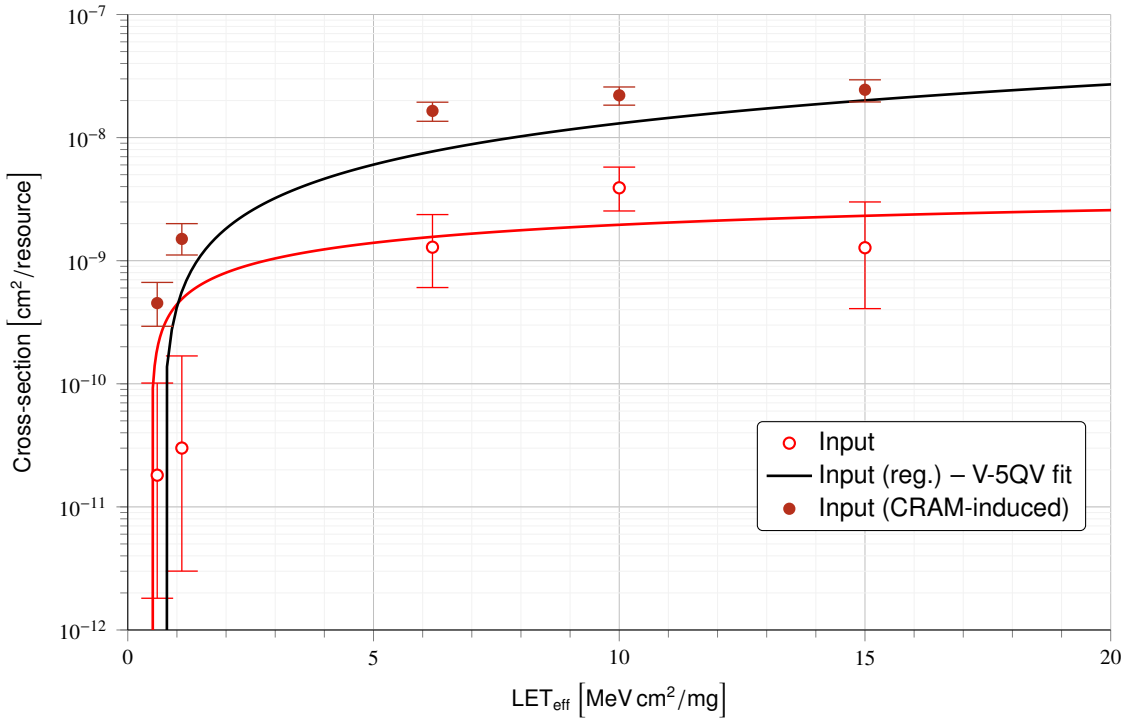


Figure 22: *Virtex-7* LVCMOS Input combined (three test variants) upset cross-sections for heavy ions. Weibull fit parameters are: $\sigma_{sat} = 3.92 \times 10^{-9}$, $L_{th} = 0.472$, $W = 17.4$, $S = 0.606$. The Weibull fit for 65nm *Virtex-5QV* registered output upsets is also plotted (fit parameters in [11]).

In a similar way, LVCMOS outputs' cross-sections are provided, for all three test variants combined. Figure 23 shows, for these combined outputs, transient and CRAM-induced upsets; also included in the figure is the Weibull fit resulting from registered output transient upsets on *Virtex-5QV* [11]. Analogous comments apply similar to the previous (inputs) case.

[TBD]: General comments. Even with short lengths of routing, enough configuration bits are involved; as a result, configuration-induced (scrub-able) errors dominate over the transient (self-recovery) type of errors. **[TBC]: Modify/remove the following sentence (we can't do this with the available data). Sebas.** These upset modes should be the same for the registered and unregistered cases and so, for data upsets, subtraction should yield the susceptibility of the register itself albeit with larger error bars.

[TBC]: Group LVCMOS test in Input-Output joint events, to be able to combine this data with the LVCMOS-MAXIO test dataset (1:1 I/O relation). Sebas.

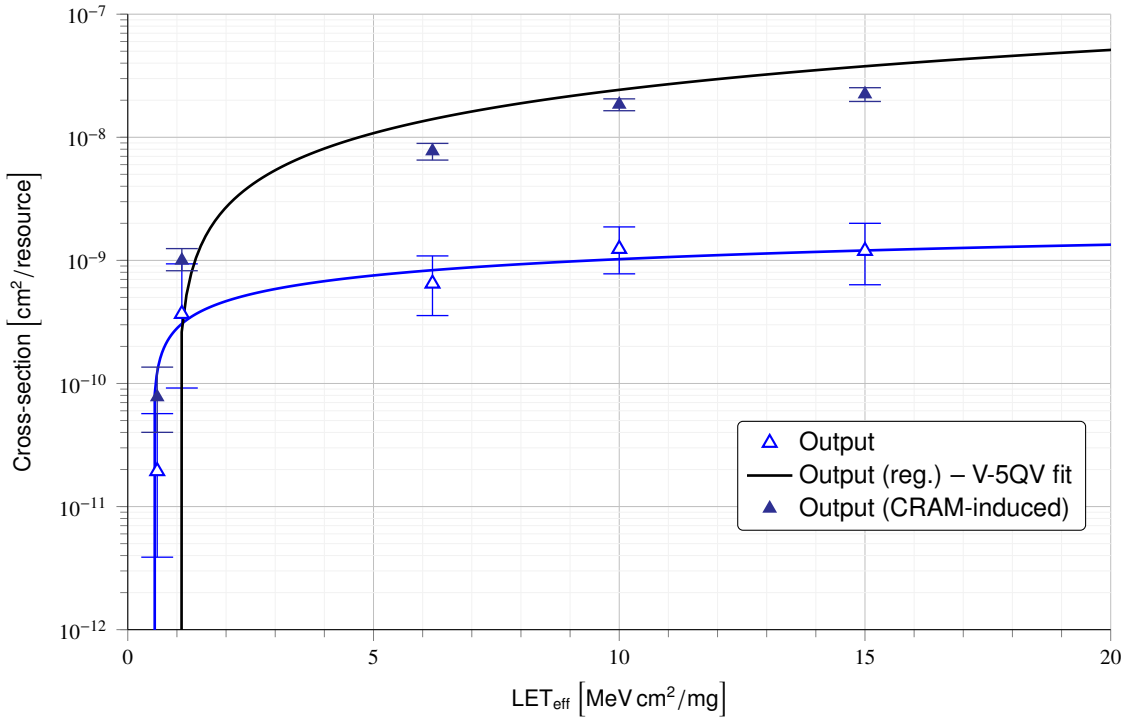


Figure 23: *Virtex-7* LVCMOS Output combined (three test variants) upset cross-sections for heavy ions. Weibull fit parameters are: $\sigma_{sat} = 3.00 \times 10^{-9}$, $L_{th} = 0.512$, $W = 57.0$, $S = 0.488$. The Weibull fit for 65nm *Virtex-5QV* registered output upsets is also plotted (fit parameters in [11]).

11.4 Results: Individual LVDS-IOBs

For the LVDS differential I/O standard, the test setup has the DUT's internal loopback implemented with one input excited by *FuncMon* directly routed to one output monitored by the same *FuncMon* FPGA[†]. Then, in this case any upset event is a joint input-output event, as we can not discriminate an upset affecting either an input or output. For the two signal frequencies, only the un-registered configuration went into the beam. Then, the test variants are here labeled as: **a) LVDS-UL:** Unregistered and Low-frequency, and **b) LVDS-UH:** Unregistered and High-frequency.

As shown in the joint input-output cross-sections of Fig. 24, for both test variants we have just a few valid data points, only for two low LET runs. The figure includes corresponding CRAM-induced upset cross-sections.

Figure 25 shows joint input-output upset cross-sections, when combining the two test variants. Again, CRAM-induced upsets are shown for the same combined tests.

11.5 Results: Individual HSTL-IOB

For the HSTL standard the available data corresponds to a single LET value on an un-registered and low-frequency test configuration.

Figure 26 shows the cross-section points for transients affecting inputs and outputs, and also the corresponding CRAM-induced upset cross section. No "classic" transient events were observed, but there are some transient anomalies present in the dataset that may suggest a new upset mode signature; more research is required on this clue. Comparing with the LVCMOS-UL test variant on Fig. 19, this scarce HSTL data is consistent with the hypothesis of no significant difference between the upset susceptibility of these two standards.

[†] As an internal reminder for the experimentalists and data analysts, in this footnote we document that the LVDS test is part of the "MAXIO" test dataset, where more than one IOB std. has been exposed to the beam on a given run.

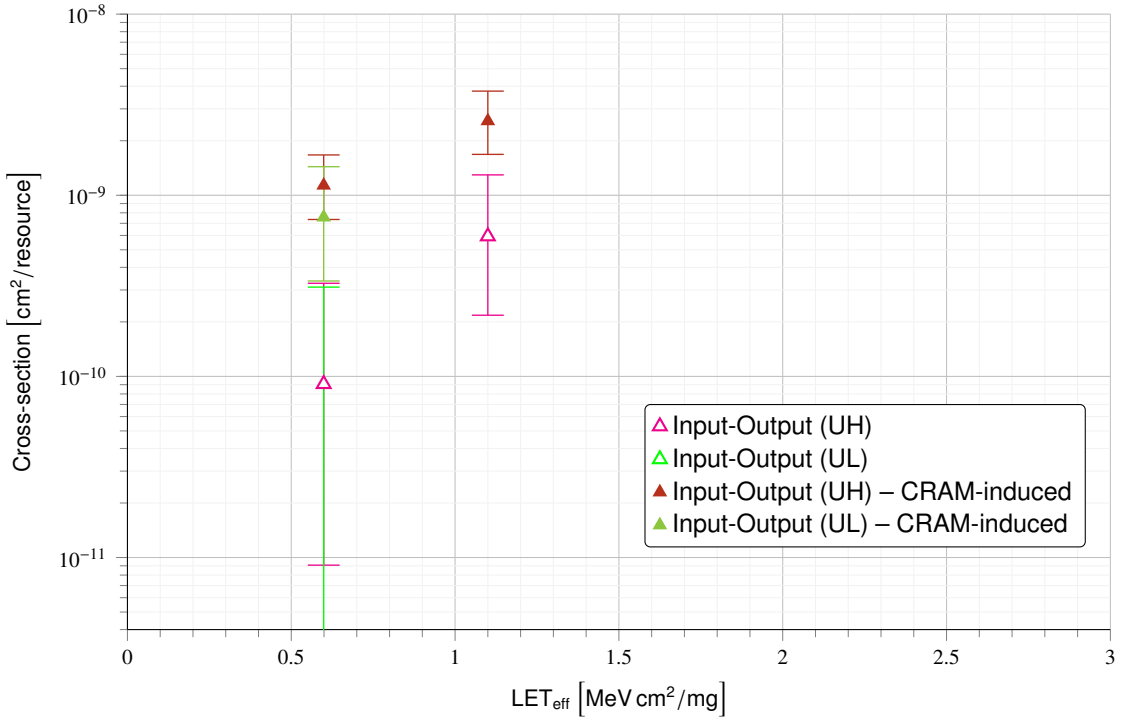


Figure 24: *Virtex-7* LVDS Input-Output joint upset cross-sections grouped in *low-* and *high-frequency*, both being *un-registered* tests. CRAM-induced upsets affecting each test variant are also shown.

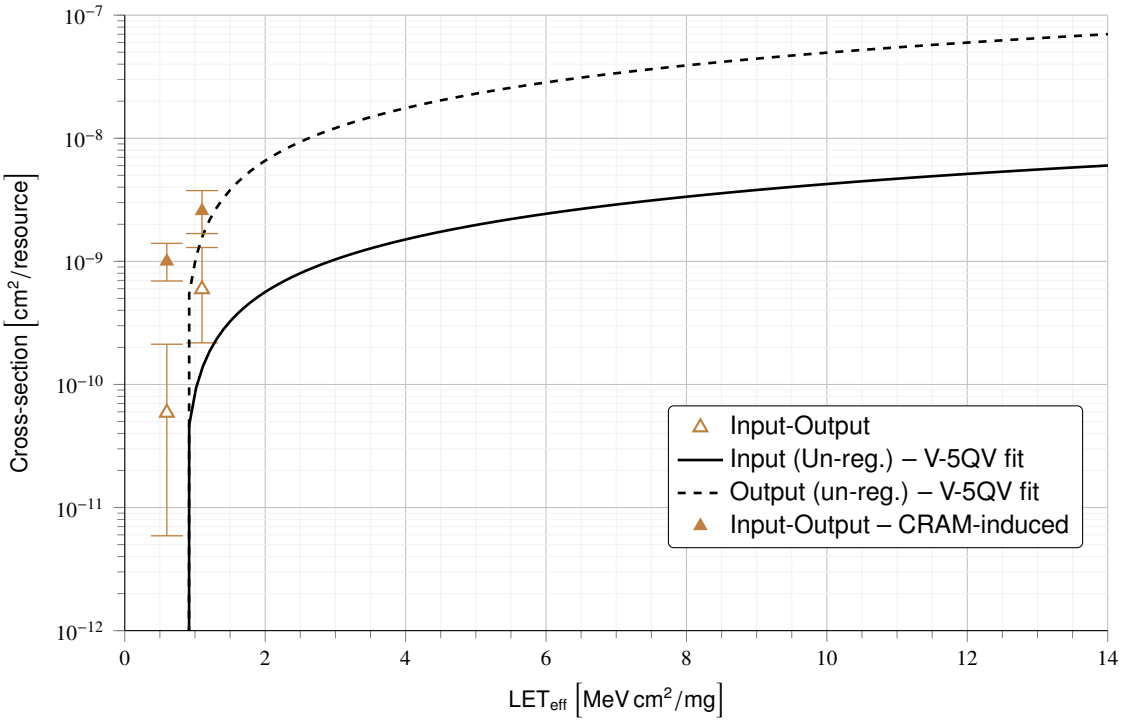


Figure 25: *Virtex-7* LVDS Input-Output joint upset cross-sections, both test variants combined. CRAM-induced upsets are also shown. Weibull fits for 65nm *Virtex-5QV* un-registered inputs and outputs are also plotted (fit parameters in [11]).

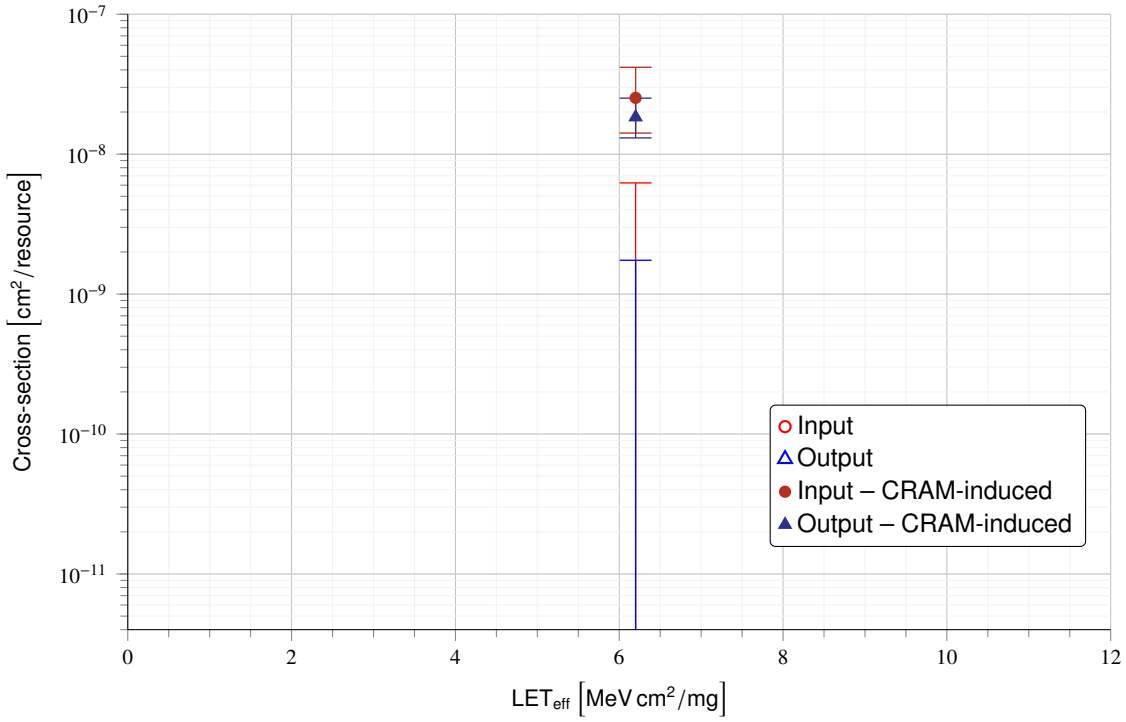


Figure 26: *Virtex-7* HSTL (*un-registered* and *low-frequency*) upset cross-section for heavy ions. CRAM-induced upsets affecting HSTL I/Os are also plotted.

11.6 Results: SERDES

The “IOSERDES” test was run with the LVCMOS I/Os and uses a similar ’loopback’ concept but involves a 4-bit bus and 4-bit de-serializer registers on inputs and 4-bit serializer registers on outputs. Again, subtraction of the unregistered LVCMOS results should yield the register susceptibility and, as before, the register bits’ cross sections are quite small. See Fig. 27 for input and output associated events, and Fig. 28 for a comparison with *Virtex-5QV*.

11.7 Results: Full IOB Banks

Here the resource considered is an entire bank of I/Os. In this context, the *per-resource cross-section* term refers to a given cross-section normalized to the total number of banks under test for the corresponding IOB standard.

Figure 29 shows experimentally-obtained cross-section points and corresponding Weibull fits. It is reasonable to assume that there’s no significant differences between the various I/O standards, because the logic that control/affects entire banks might be similar (or indeed the same). Therefore, no matter what IOB standard is actually configured, the bank upset susceptibility should be similar. As we see in Fig. 29, the available data is consistent with this assumption.

[TBC]: Re-do both Weibull fits. Sebas.

11.8 Summary

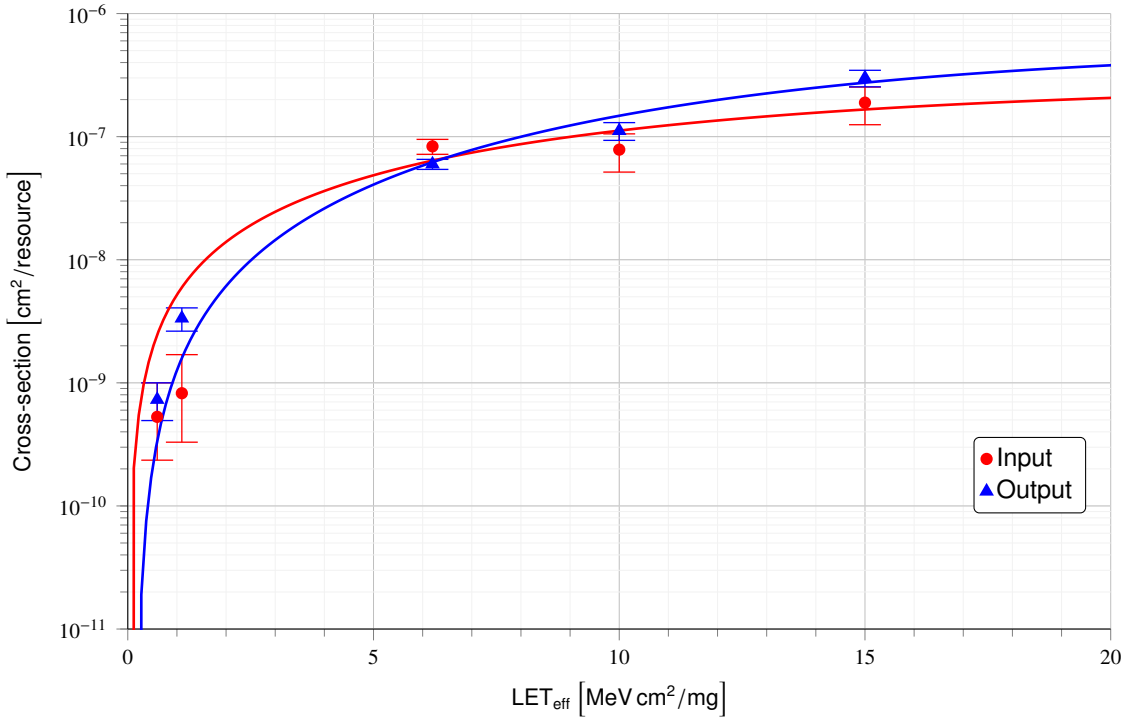


Figure 27: *Virtex-7* IOSERDES upset events associated with pins assigned as inputs or outputs. Outputs are a bit more susceptible than inputs. Weibull fit parameters are: *(a) Input:* $\sigma_{sat} = 2.71 \times 10^{-7}$, $L_{th} = 0.0224$, $W = 15.5$, $S = 1.43$; *(b) Output:* $\sigma_{sat} = 5.04 \times 10^{-7}$, $L_{th} = 0.176$, $W = 16.7$, $S = 1.99$.

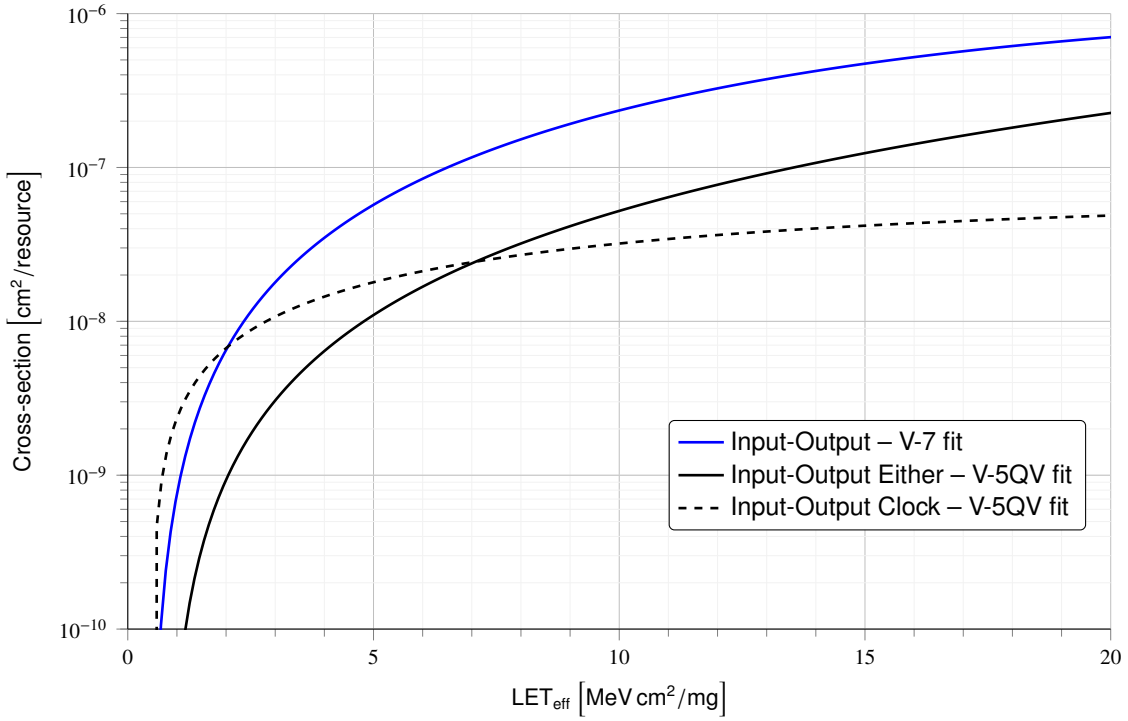


Figure 28: *Virtex-7* IOSERDES Weibull fit for joint Input-Output upset contributions. The fit parameters are: $\sigma_{sat} = 1.10 \times 10^{-6}$, $L_{th} = 0.477$, $W = 19.3$, $S = 2.02$. Also plotted are joint Input-Output upsets modes seen during *Virtex-5QV* campaign (fit parameters in [11]).

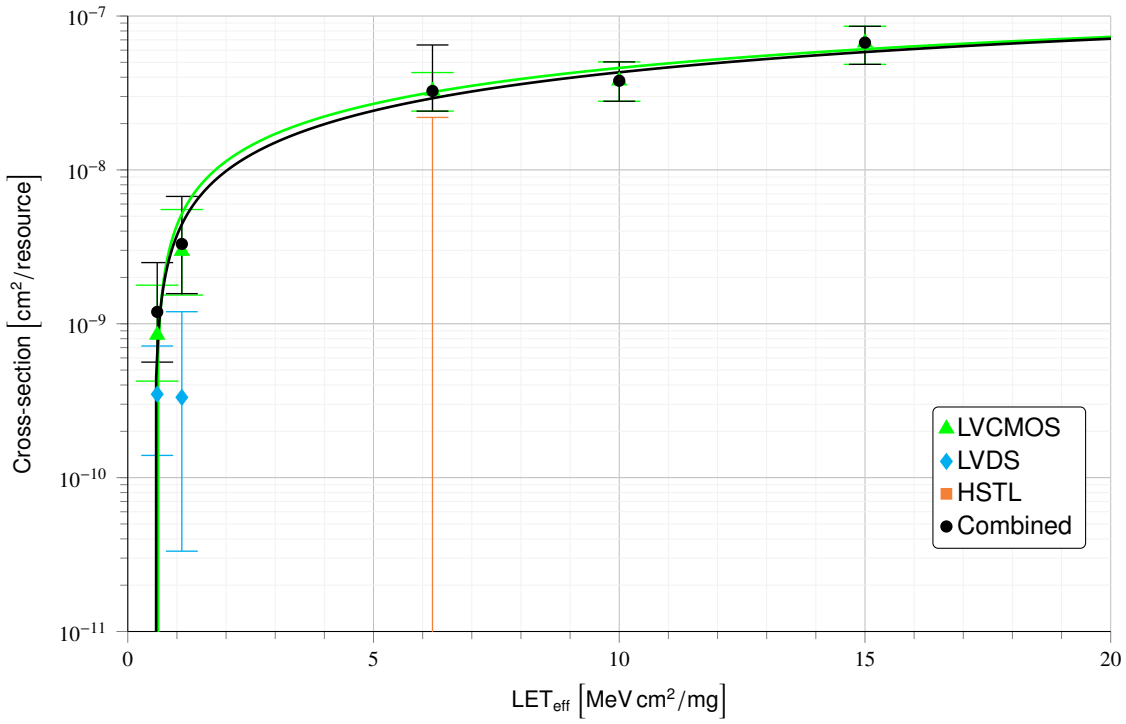


Figure 29: *Virtex-7* IOB Bank upset cross-sections. For the corresponding Weibull fit curves, the associated parameters are: *(a) LVCMOS:* $\sigma_{sat} = 1.69 \times 10^{-7}$, $L_{th} = 0.581$, $W = 39.5$, $S = 0.801$; *(b) Combined:* $\sigma_{sat} = 1.78 \times 10^{-7}$, $L_{th} = 0.541$, $W = 43.1$, $S = 0.848$.

12 BRAM and BRAM-ECC Test Results

– William J. Rowe – Raytheon Space and Airborne Systems, El Segundo, CA, USA –

12.1 Introduction

Like with the CRAM cross-section, the *Block RAM* bit upsets results on *Kintex-7* published in [1] should in principle directly apply to *Virtex-7* as well. The BRAM components used in Virtex and Kintex 7 devices consists of identical circuitry, layout, and was manufactured in the same process. However, during BRAM testing, discovered this to not be the case.

Logic components such as the facilities ECC usage as well as port parameters are configurable.

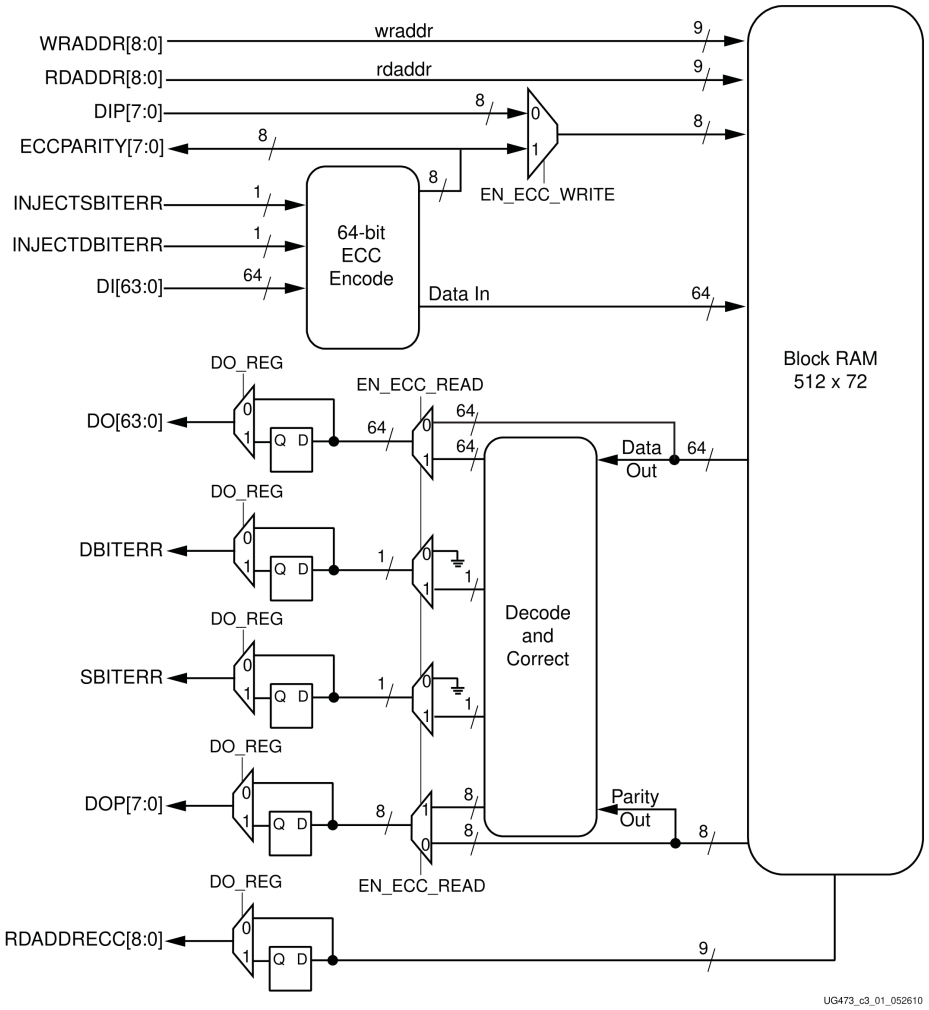


Figure 31: A Virtex-7 BRAM primitive including peripheral logic but without SRAM cascading.

12.2 Test Methodology and IP

The BRAM test can be done in the following ways: - Static manner: We load pattern before the beam goes on, and do the upset readback after the beam goes off. - Pseudo-static manner: We hit the read button through the radiation, so we keep it busy reading and looking for errors. - Dynamic manner: The design reads all BRAMs all the time. This was only done in some of the last runs of TAMU 2017.03 (previously not working).

non-ecc was conducted as a static test and was performed during all 3 beam trips

bram-ecc was a dynamic test, but only done the later 2 trips, because the dut/funcmon design did not work

ECC port width 72bit

non-ECC port width 36bit

Precursor IP was bramx greg r allen/JPL from the v5 report

all BRAMs connected via shared data/address bus and directly controlled by funcmon design

The DUT and *FuncMon* HDL designs previously used for testing *Virtex-5QV* IOB and BRAM-ECC were adapted to the V7-585T and V7-980T DuT devices. For comparison purposes, the BRAM IP was also ported to the two *Virtex-7* DUTs.

The general test setup for both BRAM and BRAM with Error Correcting Code (ECC) module is as follows. All the 795 BRAM blocks under test are initialized with a bit pattern (checkerboard for most of the runs) in each word position. For each BRAM, there is a sequential read of data words, operating circularly. For the BRAM-ECC test, in case of a single-bit error found after a given word read, the corrected word is presented at the ECC module's output and an immediate write-back to that memory position is performed by the test code, in order to correct the corrupted bit in the storage cell.

When testing with ECC, BRAM blocks were read continuously while being exposed to the beam. Any mismatch between what was read and what had been initially written to the BRAM blocks was recorded as an error. Testing done without ECC read the contents of the BRAM blocks after exposure to the beam ended and then compared to what was initially written to the BRAM blocks.

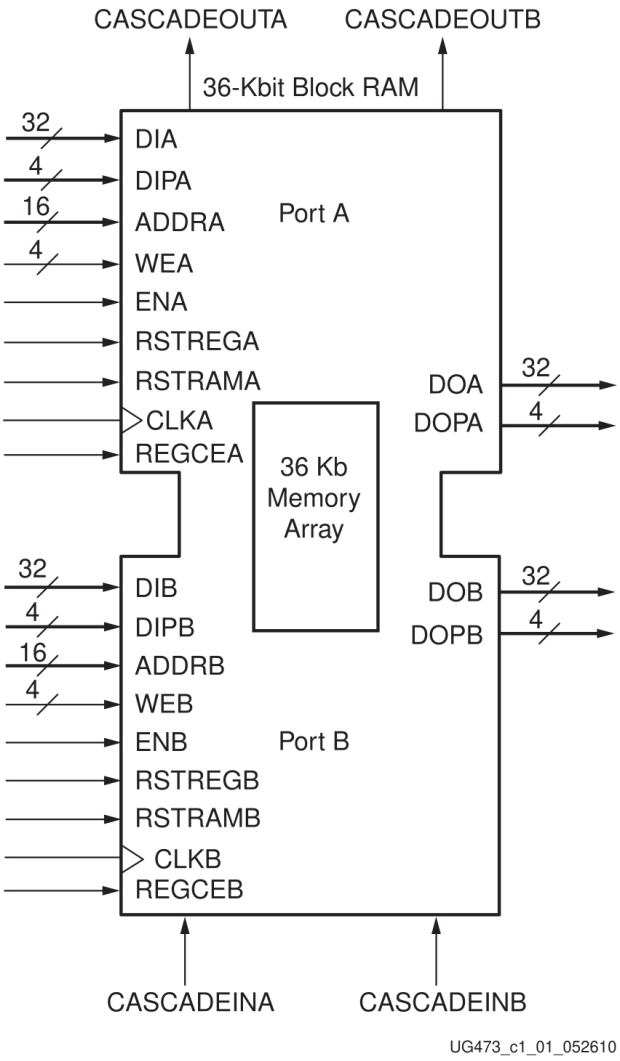


Figure 32: A true dual-port block memory on Virtex-7 including up-/downwards cascading signals.

A (72, 64) Hamming (distance 4) code based Single-Error Correction and Double-Error Detection (SECDED) ECC module is available inside each BRAM block, as an Error Detection and Correction (EDAC) scheme to mitigate memory cell upsets and significantly reduce the errors that result. Each BRAM block available in the

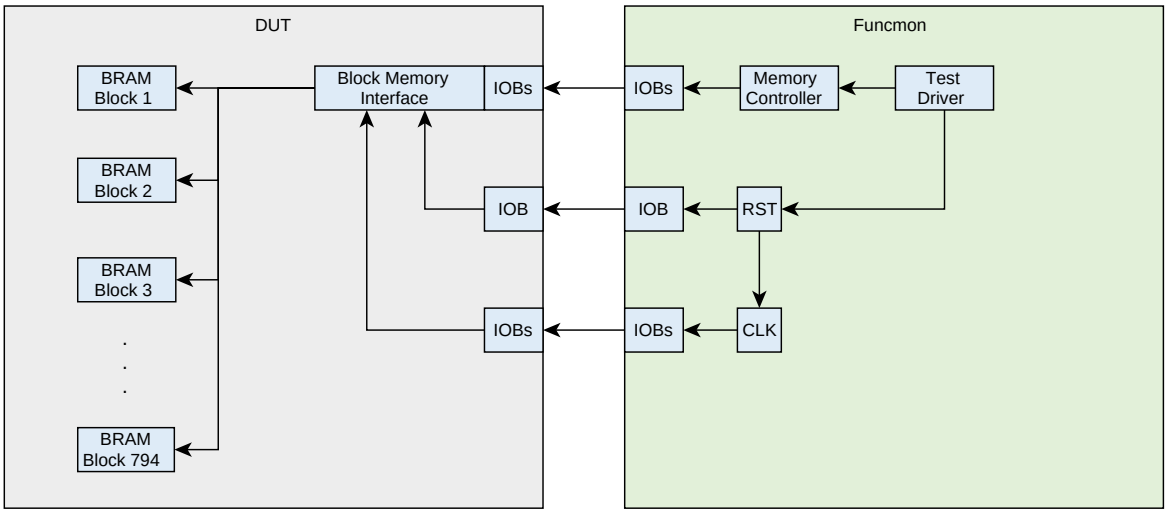


Figure 33: The V-7 BRAM/BRAM-ECC DUT design.

DUT is configurable as 512 64-bit data words, in addition to 8-bit ECC check bits (parity) for every data word. During a write condition, the corresponding byte of check bits is generated and stored together with the data into an overall 72-bit word. During a read operation this Hamming-encoded 72-bit word is fed into the ECC decoder to detect and correct (on the ECC output) single-bit errors, and detect (but not correct) double-bit errors. The decoder generates status outputs indicating: no error, single-bit error detected and corrected, or double-bit error detected. The BRAM cells are implemented such that logically adjacent bits in a given word are physically interleaved within logically adjacent bits in a different word. This physical interleaving of the memory cells is an effective technique to mitigate the possibility of any MCU appearing as an MBU upset and defeating the SECDED scheme.

12.3 Results: BRAM Bit Errors Patterns

The results obtained in the XRTC Virtex-7 beam trips demonstrate non-Poisson accumulation over the course of each run. The per *Block RAM* cross-section for bit position modification events (BBPM) are shown in Fig. 34. Careful analysis of the data reveals that a control SET occurs occasionally flipping 1024 bits, one per 36-bit word in a particular 36 Kbit block. Logically, the bits flipped are all in the same bit position for each address in the block, hence they are dubbed *Block RAM* bit position modification (BBPM) single events.

These BBPM events were seen after exposure to particles stopped and are clearly persistent bit flips.

In addition to BBPM events, other instances of non-Poisson accumulation were observed where 512 bits, one per 72 bit word. These events are seen when reviewing logs of error counts recorded while the test device was being exposed to particles. However, contents of BRAM after the particle exposure ended did not show these events, indicating these are transient events. Also, the counter recording the number of bits corrected by ECC did not show instances where 512 bits were corrected in one bit position. So, it is assumed these events are likely the result of an addressing error. Due to the way bit flips were recorded, it is unclear how many instances of events with 512 bits flipped in one bit position occurred in any given test run.

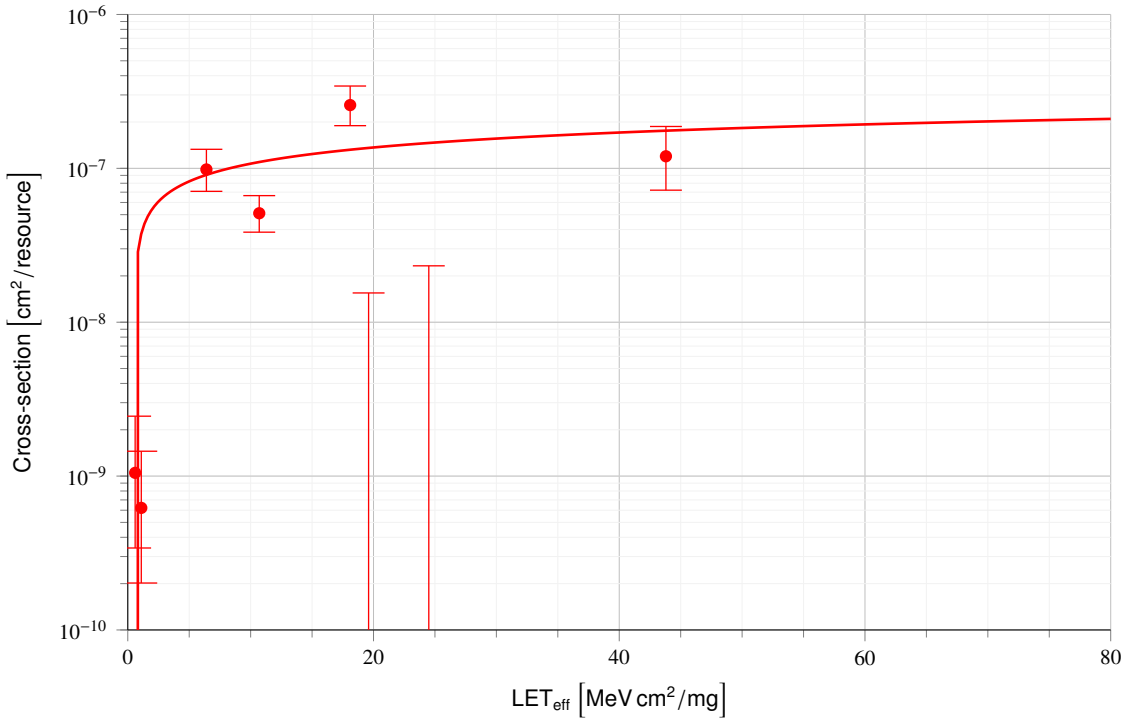


Figure 34: *Virtex-7 Block RAM* bit position modification (BBPM) events. Weibull fit parameters are: $\sigma_{sat} = 4.2 \times 10^{-7}$, $L_{th} = 0.56$, $W = 200$, $S = 0.4$.

12.4 Results: ECC Performance

The ECC performance for BRAM primitives was verified using data obtained during the January 2017 proton beam test and the March 2017 heavy ion beam test. No ECC radiation data was collected during the December 2016 heavy ion beam trip, as the original design used back then was non-functional and could be reworked in time for the January 2017 beam trip.

The obtained data as well as fitted Weibull curves are depicted in Fig. 36. The dashed line shown in Figure 36 represents a "fitting by inspection" of the data points, confirming the expected quadratic dependence of the system error rate on the raw bit flip rate. The extracted fitting parameter is consistent with the cycle time of the JCM used during the test of $T_C \simeq 25s$. For this scrubbing time we obtain $EWER = (0.5{*}25{*}795{*}512{*}72{*}71){*}Rbf^2$

System error is defined either as an EDAC word error (two or more bit errors in a single word) or an anomalous failure in the EDAC system. *Virtex-7* BRAM-ECC results show that uncorrectable double-bit errors (whether from MCUs or coincident SBUs) are lowered by 2+ orders of magnitude from the BRAM upsets (shown here as correctable single-bit errors) even at the high fluxes used in heavy ion testing. Proton test results closely matched heavy-ion test results. In addition, one 512-bit column hit event was noted.

The underlying upset rate of BRAM is reduced by approximately a factor of two relative to the beam flux. The corresponding coincidental error rate is decreased by a factor of four, and in absolute terms several orders of magnitude lower. The ECC performance thus follows a Poisson-derived quadratic relationship of effective mitigation. The results therefore verify Edmonds' law for system error mitigation [16].

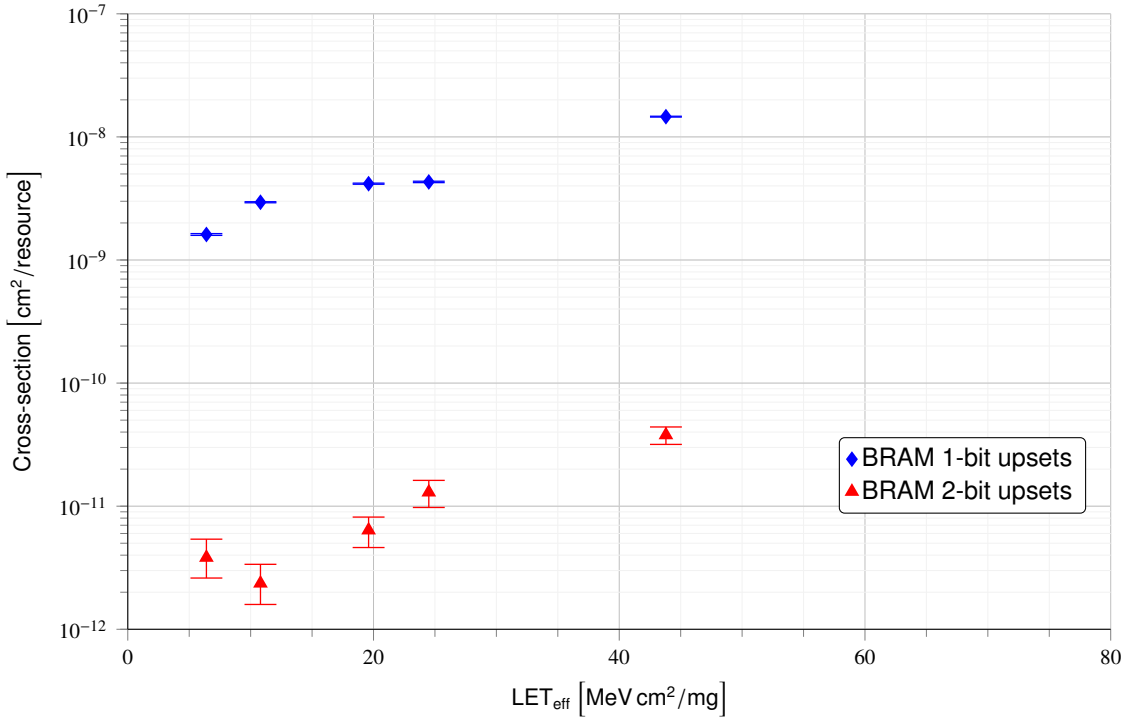


Figure 35: Relation between BRAM-ECC correctable 1-bit error and detectable but uncorrectable 2-bit error rates obtained for the *Virtex-7* devices.

12.5 Summary

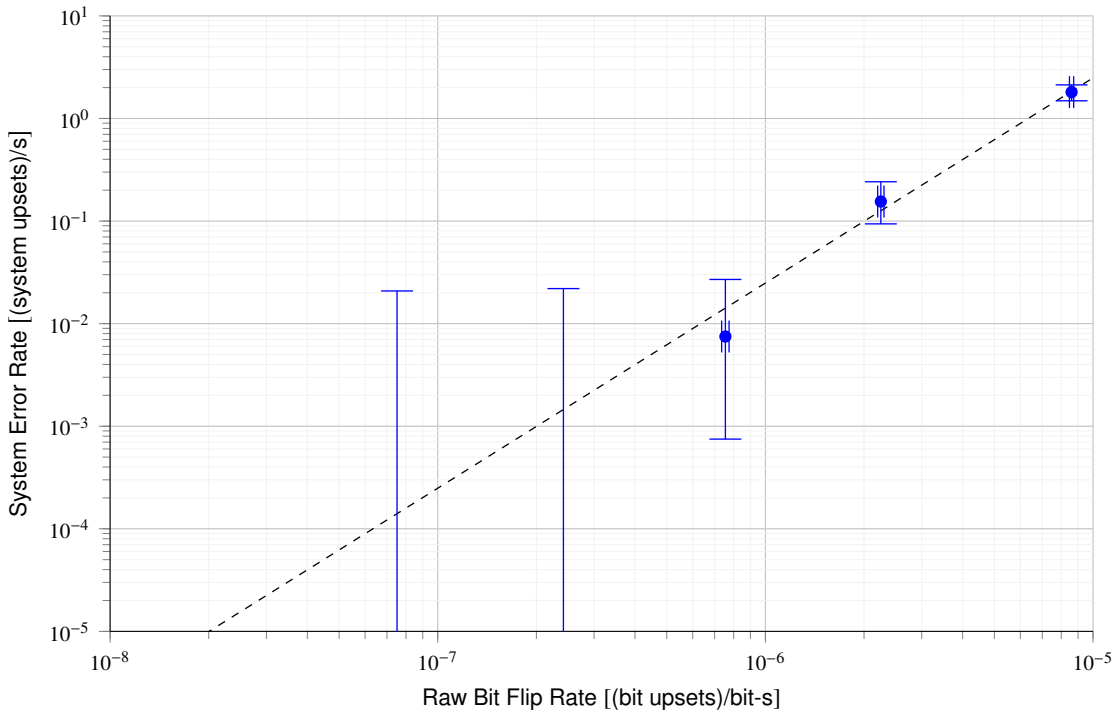


Figure 36: *Virtex-7* BRAM-ECC block behavior under proton irradiation.

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13 Single Event Functional Interrupts

13.1 Introduction

The large fluences used for counting low probability dynamic upsets for the Virtex-7 FPGAs in the test campaign yielded an abundance of test data. The XRTC Series-7 radiation test campaign allowed us to test a very broad variety of fabric components found in FPTAs of this generation. This allows us to also characterize the overall SEFI cross section of Series-7 devices. The relevant data and SEFI-related Weibull fits are presented in this section.

In contrast to prior tests carried outby D.S. Lee et al. in [1], we can do so now based on considerably more Single-Event Functional Interrupt (SEFI)-related data with a very broad component coverage and with much higher fluences. In this section, we mainly utilize data obtained in the two heavy ion tests conducted in the TAMU cyclotron in December 2016 and March 2017.

[CF to Bill]: I see no mention of SEFI results from proton testing. What about that? Or just too little data? Or nobody did it?

13.2 Test Methodology and IP

We utilize a superset of all data accumulated for CRAM and in the tests for clocking resources, IOBs, and BRAM related components. This data was combined, which yielded an abundance of SEFI-related data. Hence, in contrast to tests described in the other sections of this report, no dedicated test setups had to be developed or testing to obtain this data. The analysis carried out in this section therefore considers high-level device behavior purely related to SEFI-like faults.

For Xilinx Series-7 devices, we observed the following SEFI signatures:

- Power-On-Reset (POR) – SEFIs directly or indirectly resulting in a global reset the FPGA's CRAM.
- SMAP Upset (SU) – SEFIs causing a loss of correct functionality for the SelectMAP interface.
- Global Signal (GSIG) – SEFIs that cause the DUT's IOBs and other IO signals to be driven to a HIGH or LOW state.

In [17], we included several additional SEFI types. However, according to the obtained data no significant results were obtained that could be classified in those categories.

13.3 Results: Component SEFI Cross-Section

Considering the IO distribution of the tested V7-980T and V7-585T FPGAs, we expect to see primarily POR and GSIG SEFIs. The silicone-footprint share of I/O-resources dedicated to an SMAP interface is much smaller, hence SU SEFIs should be drastically rarer than the other types.

In Fig. 37 we present SEFI components identified from heavy-ion testing up an effective LET of 80 MeV. From this data and the achieved Weibull fits, we see that indeed, a large majority of all SEFIs encountered with Virtex-7 devices manifests as POR and GSIG upsets. POR and GSIG SEFIs dominate by 1 and 2 orders of magnitude, respectively, as compared to SU Upsets.

Analyzing just the lower LET range of the Weibull fits depicted in Fig. 38, we can see that For SE SEFIs, the fit Weibull curve flattens already above an LET of 5MeV, as is the case for GSIG SEFIs above 10MeV. The cross section of POR SEFIs increases gradually with rising fluence.

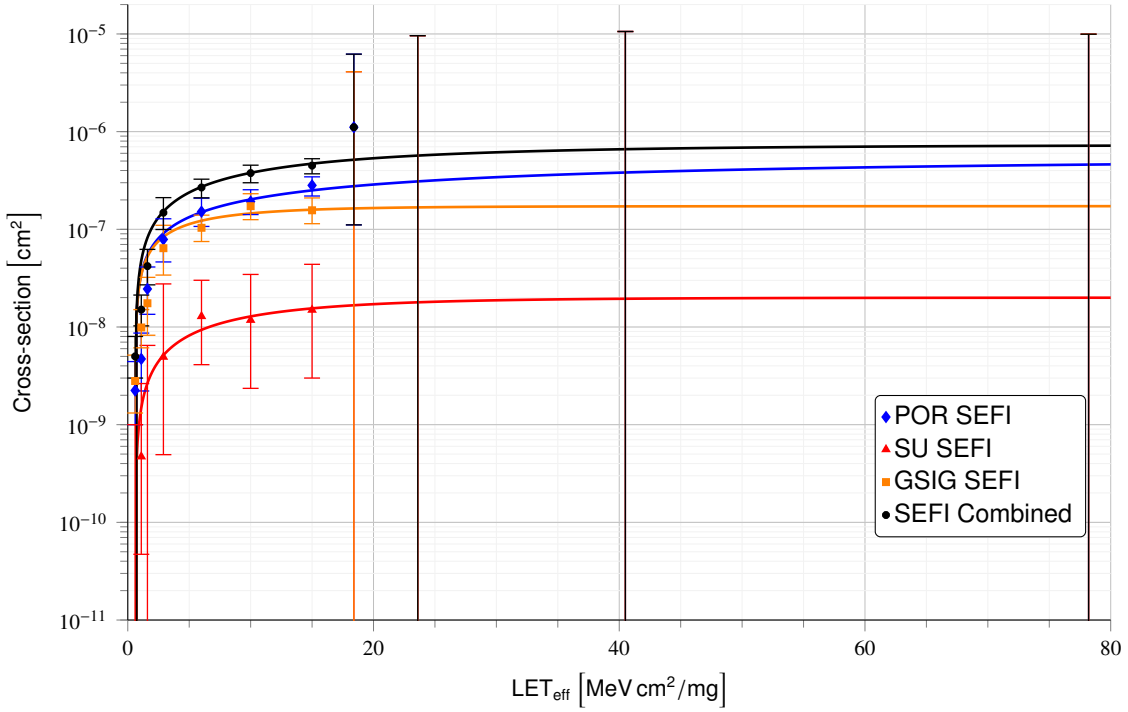

Figure 37: *Virtex-7* SEFI events, showing individual and combined contributions. Weibull fit parameters are: *(a) POR:* $\sigma_{sat} = 5.39 \times 10^{-7}$, $L_{th} = 0.598$, $W = 29.2$, $S = 0.665$; *(b) SU:* $\sigma_{sat} = 2.00 \times 10^{-8}$, $L_{th} = 0.599$, $W = 9.10$, $S = 0.881$; *(b) GSIG:* $\sigma_{sat} = 1.73 \times 10^{-7}$, $L_{th} = 0.585$, $W = 4.06$, $S = 0.733$; *(d) Combined:* $\sigma_{sat} = 7.31 \times 10^{-7}$, $L_{th} = 0.599$, $W = 13.9$, $S = 0.810$.

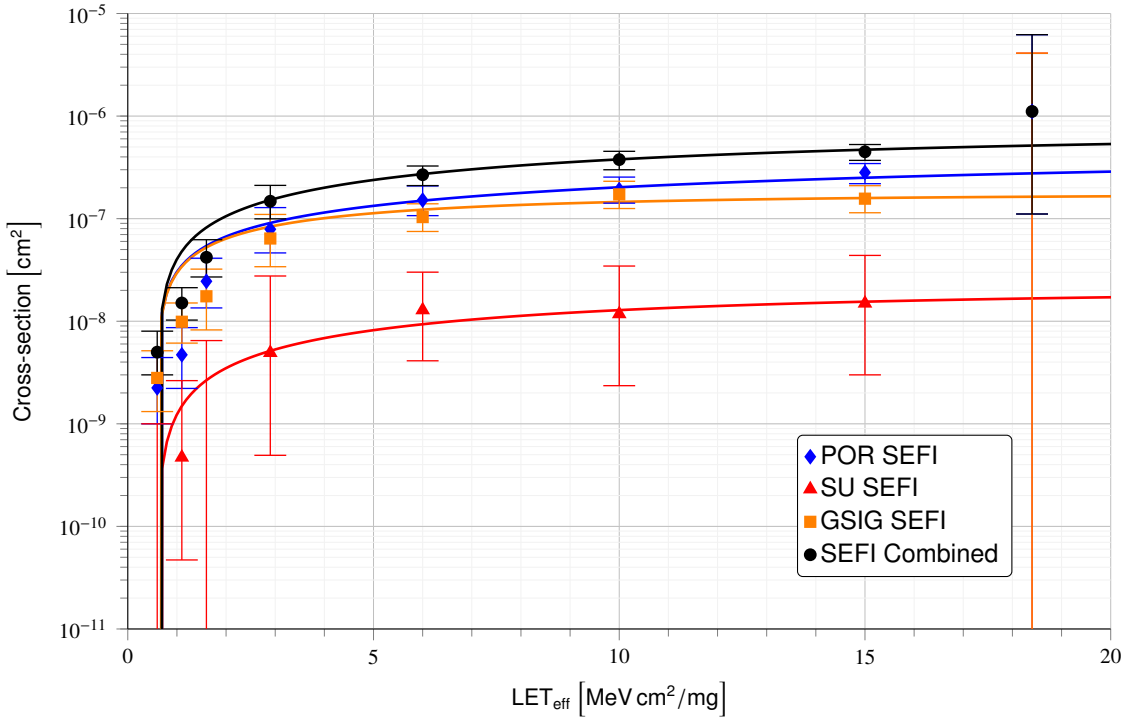

Figure 38: *Virtex-7* SEFI events, showing individual and combined contributions. Same plot as in Fig. 37, now with more detail for low LETs.

13.4 Results: Comparison to V-5QV

Figure 39 shows a comparison with *Virtex-5QV* results [10].

[CF to Gary]: What's the take home message for a reader here? The difference in cross section between V7 and V5 at low LETs is still comparable to that with the cross-section difference for CMT SEU between V5 and V7. ?

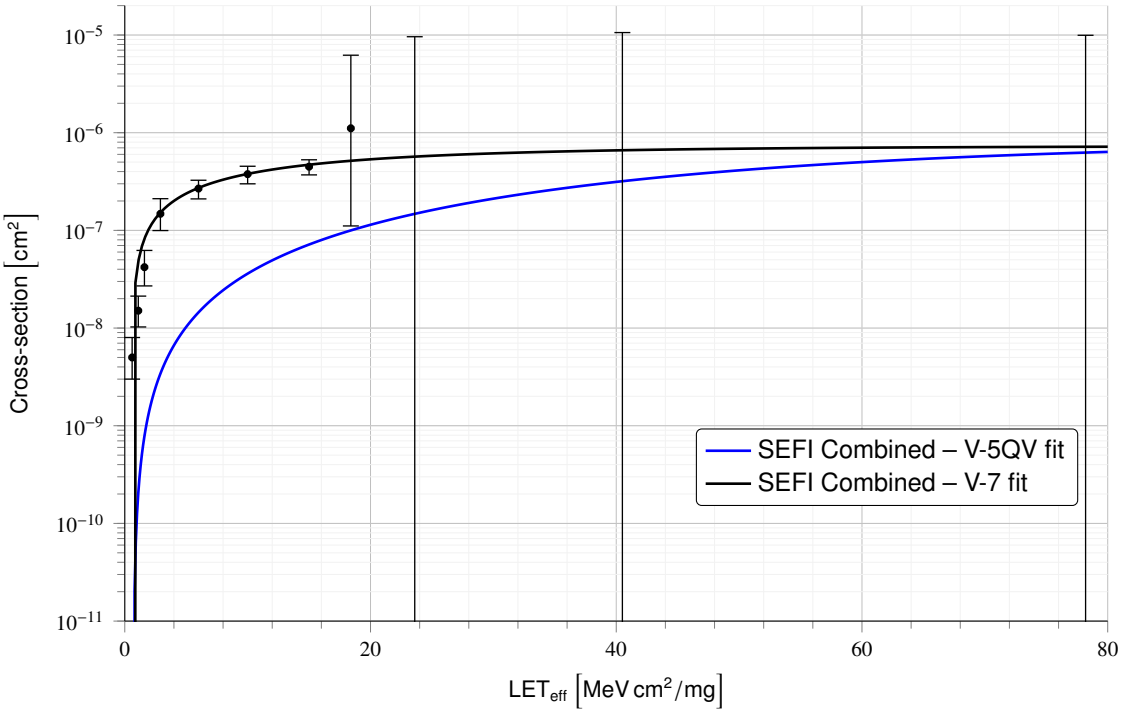

Figure 39: Cross-sections of *Virtex-7* POR, SU, GSIG contributions to SEFI combined, compared with *Virtex-5QV* SEFI result.

[TODO for Bill]: Add side-by-side comparison between V5 and V7 Weibull fits and whisker-plots for

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14 Space SEE Upset Rates

Heavy ion upset rates in the table below were computed for the orbits indicated using the method outlined in JPL Publication 91-32 with the thickness to radius ratio set to 0.2. The input flux was computed using CREME96 with the following conditions:

- Solar minimum
- Z_{min} set to 2
- 100 mils aluminum shielding

The method in JPL Publication 91-32 comnputes the final rate by replacing the fitted Weibull curve with a bounding stair step curve. The rates in the table below are the average of bounding stair step curve and the stair step curve bounded by the Weibull curve removing some conservatism.

Resource	**LEO (low)** 500 km 22.0°	**LEO (mid)** 800 km 51.6°	**LEO (high)** 1200 km 65.0°	**Polar** 833 km 98.7°	**GEO**	**GPS** 20200 km 55.0°
MMCM Single	3.64×10^{-5}	1.17×10^{-5}	7.5×10^{-5}	8.43×10^{-5}	2.49×10^{-4}	2.36×10^{-4}
MMCM Instance	9.3×10^{-6}	2.97×10^{-6}	1.94×10^{-5}	2.18×10^{-5}	6.50×10^{-5}	6.14×10^{-5}
MMCM Global	3.95×10^{-7}	1.24×10^{-7}	8.39×10^{-7}	9.54×10^{-7}	2.88×10^{-6}	2.72×10^{-6}
PLL Single	3.02×10^{-5}	9.44×10^{-6}	6.41×10^{-5}	7.26×10^{-5}	2.18×10^{-4}	2.06×10^{-4}
PLL Instance	9.26×10^{-6}	2.89×10^{-6}	1.96×10^{-5}	2.22×10^{-5}	6.68×10^{-5}	6.31×10^{-5}
PLL Global	3.53×10^{-7}	1.06×10^{-7}	7.76×10^{-7}	8.94×10^{-7}	2.76×10^{-6}	2.60×10^{-6}
GSIG SEFI	1.65×10^{-6}	5.21×10^{-7}	3.44×10^{-6}	3.88×10^{-6}	1.16×10^{-5}	1.09×10^{-5}
SU SEFI	2.47×10^{-8}	6.87×10^{-9}	5.86×10^{-8}	6.98×10^{-8}	2.27×10^{-7}	2.12×10^{-7}
POR SEFI	1.78×10^{-6}	5.61×10^{-7}	3.74×10^{-6}	4.24×10^{-6}	1.27×10^{-5}	1.20×10^{-5}
SERDES input	6.30×10^{-7}	1.80×10^{-7}	1.46×10^{-6}	1.72×10^{-6}	5.52×10^{-6}	5.16×10^{-6}
SERDES output	2.94×10^{-7}	9.17×10^{-8}	6.20×10^{-7}	7.03×10^{-7}	2.12×10^{-6}	2.00×10^{-6}
LVDS	1.41×10^{-7}	4.41×10^{-8}	2.91×10^{-7}	3.28×10^{-7}	9.71×10^{-7}	9.16×10^{-7}
Register	3.58×10^{-9}	9.47×10^{-10}	8.88×10^{-9}	1.08×10^{-8}	3.61×10^{-8}	3.35×10^{-8}
BRAM	1.38×10^{-9}	2.50×10^{-10}	4.29×10^{-9}	5.61×10^{-9}	2.08×10^{-8}	1.90×10^{-8}
CRAM	1.15×10^{-8}	3.62×10^{-9}	2.42×10^{-8}	2.74×10^{-8}	8.21×10^{-8}	7.74×10^{-8}

15 Conclusions

By far most of the upset-induced errors observed were cleared by configuration scrubbing. Thus, the predominant response mode turned out to be essentially an exercise in counting how many configuration bits are involved with each feature as tested. This means that transients and register upsets, while clearly present, may be neglected in most cases; nevertheless, these results allow their separate calculation. Further, the nonconfiguration bit error susceptibility of the tested features is near or below the device SEFI susceptibility. Therefore, for unregistered or registered IOBs operating as any of LVCMOS, LVDS, or HSTL, for IOSERDES, for both digital and PLL clocking resources, and for BRAM-ECC, the measured upset susceptibility is low enough that none of these features is likely to be a significant impediment to projects and missions seeking to use the *Virtex-7* in space applications.

Appendices

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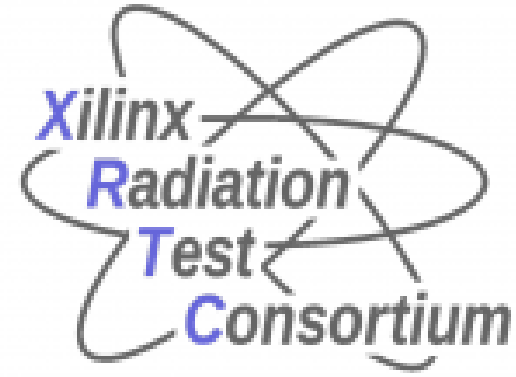
A (Placeholder for first appendix section)

A.1 (Placeholder for first appendix SUBsection)



About XRTC

The Xilinx Radiation Test Consortium (XRTC), originally known as the Single-Event Effects (SEEs) Consortium, was founded in 2002 by Caltech-NASA's Jet Propulsion Laboratory (JPL) and Xilinx to evaluate reconfigurable, SRAM-based FPGAs for aerospace applications. XRTC brings together experts from industry, government, and academia, to combine efforts towards independent and unbiased: characterization by means of radiation testing, study of upset modes, development of mitigation techniques, fault-injection simulation/emulation, complex systems (e.g., SoCs) evaluation, and methods to qualify FPGA applications for space environments.